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# INTEL® COMMUNICATIONS ICH VALUE APPLIANCE REFERENCE DESIGN REV 1.0

## UNIVERSAL DESIGN

THIS DESIGN DOES NOT CONTAIN AN SIO  
PLEASE NOTE MANY OPERATING  
SYSTEMS NEED AN SIO WITH KEYBOARD  
CONTROLLER FOR THE KEYBOARD  
TO OPERATE CORRECTLY

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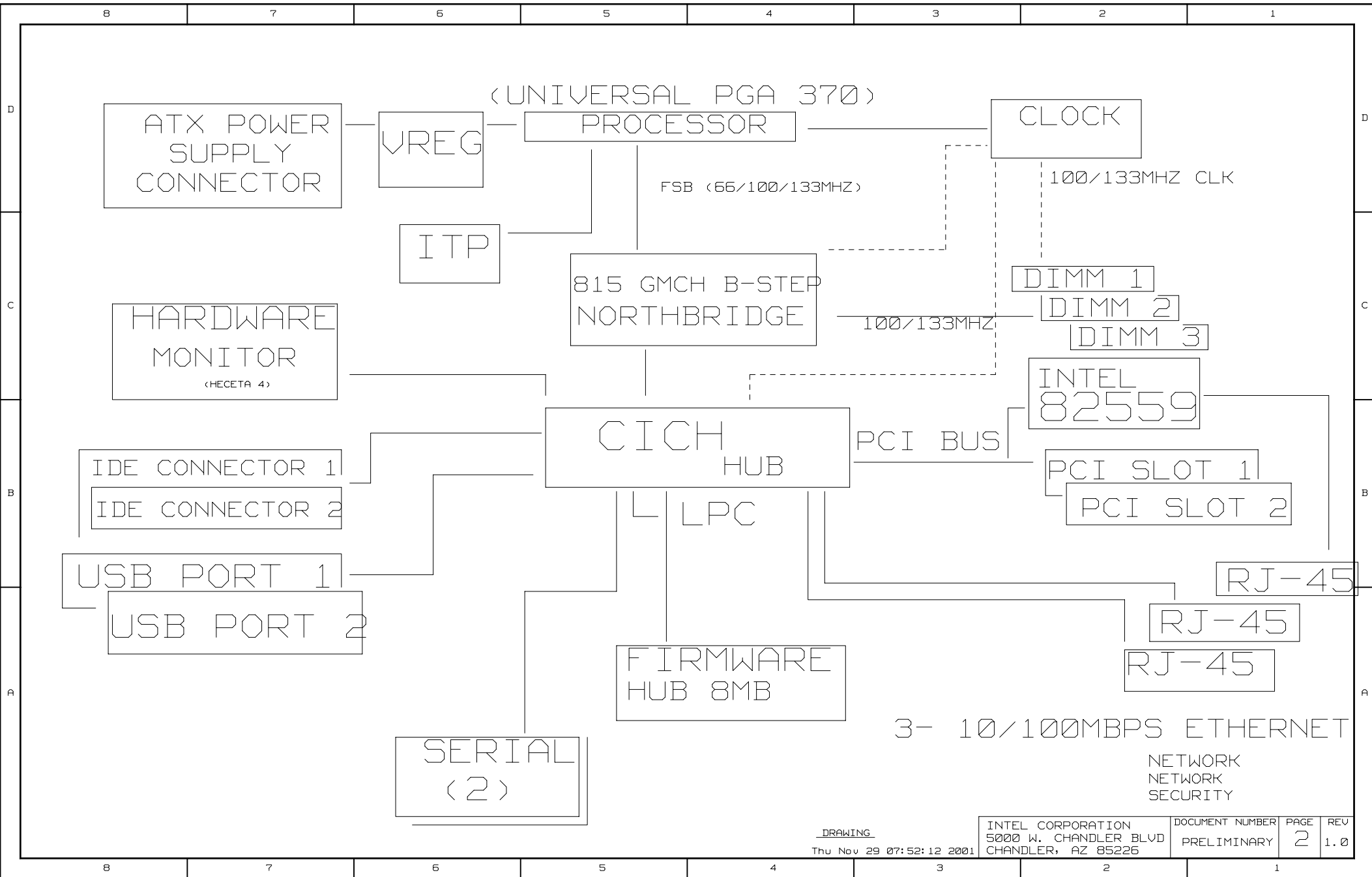
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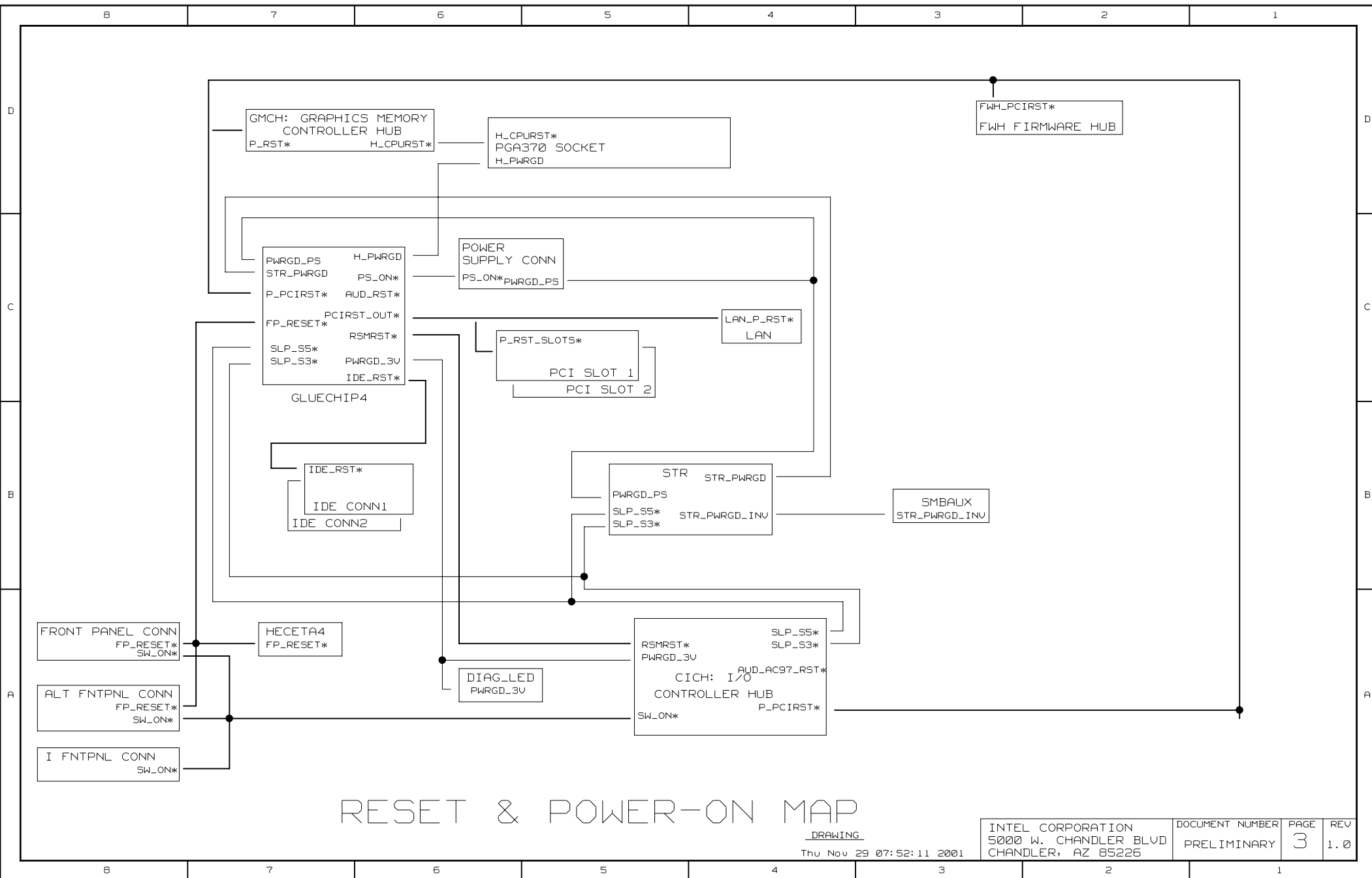
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DEVICE	BUS ID		FUNCTION	IDSEL	REQ/GNT	INTERRUPT
B2B15 GMCH						
MCH	0	1130	-	-	-	-
AGP-CNTRL	0	1131	-	-	-	-
INT GFX	0	1132				
		DEVICE ID				
-CICH						
HUB-PCI BRIDGE	0	30	0	N/A	N/A	N/A
LPC BRIDGE	0	31	0	N/A	N/A	N/A
IDE CONTROLLER	0	31	1	14	N/A	14 OR 15
USB CONTROLLER	0	31	2	18	N/A	D
SBUS CONTROLLER	0	31	3	17	N/A	B
D101 LAN 0	1	0B	0	24	N/A	E
D101 LAN 1	1	09	0	25	N/A	F OR E
B2559 LAN	X	01	0-7	17	4	D
PCI SLOT 1	X	10	0-7	26	0	A, B, C, D
PCI SLOT 2	X	11	0-7	27	1	B, C, D, A
-DEVICE 0		0		AD16	0	
-DEVICE 1		1		AD17	1	
-DEVICE 2		2		AD18	2	
-DEVICE 3		3		AD19	3	
-DEVICE 4		4		AD20	4	
-DEVICE 5		5		AD21	5	
-DEVICE 6		6		AD22	6	
-DEVICE 7		7		AD23	7	
-DEVICE 8		8		AD24	8	
-DEVICE 9		9		AD25	9	
-DEVICE 10		10		AD26	10	
-DEVICE 11		11		AD27	11	
-DEVICE 12		12		AD28	12	
-DEVICE 13		13		AD29	13	
-DEVICE 14		14		AD30	14	
-DEVICE 15		15		AD31	15	

\* ALL EXTERNAL DEVICES MAY BE ON PCI BUS X DEPENDING ON BIOS

DEVICE	NAME	I/O	POWER WELL	DURING RESET	AFTER RESET	S1	S3	S5	USAGE
CICH	GPIO[6]	I	CORE						GPIO_GRN_BLNK
CICH	GPIO[7]	I	CORE						GPIO_YLW_BLNK
CICH	GPIO[8]/LDRQ[1]#	I	RESUME						
CICH	GPIO[12]	I	RESUME						DMA66_DETECT_PRI#
CICH	GPIO[13]	I	RESUME						DMA66_DETECT_SEC#
CICH	GPIO[21]	O	CORE	HIGH	HIGH	DEFINED	OFF	OFF	GPIO_FLUSH_CACHE#
CICH	GPIO[22]	O	CORE	LO	LO	DEFINED	OFF	OFF	GPIO_MEM_SPD_WE#
CICH	GPIO[23]	O/D	CORE	LO	LO	DEFINED	OFF	OFF	
CICH	GPIO[25]/SUSSTAT#	O	CORE	HIGH	HIGH	DEFINED	DEFINED	DEFINED	
CICH	GPIO[27]	I/O/D	RESUME	LO	LO	DEFINED	DEFINED	DEFINED	
CICH	GPIO[28]	I/O/D	RESUME	LO	LO	DEFINED	DEFINED	DEFINED	

INTERRUPT AND GPIO MAP AND SYSTEM PARTS

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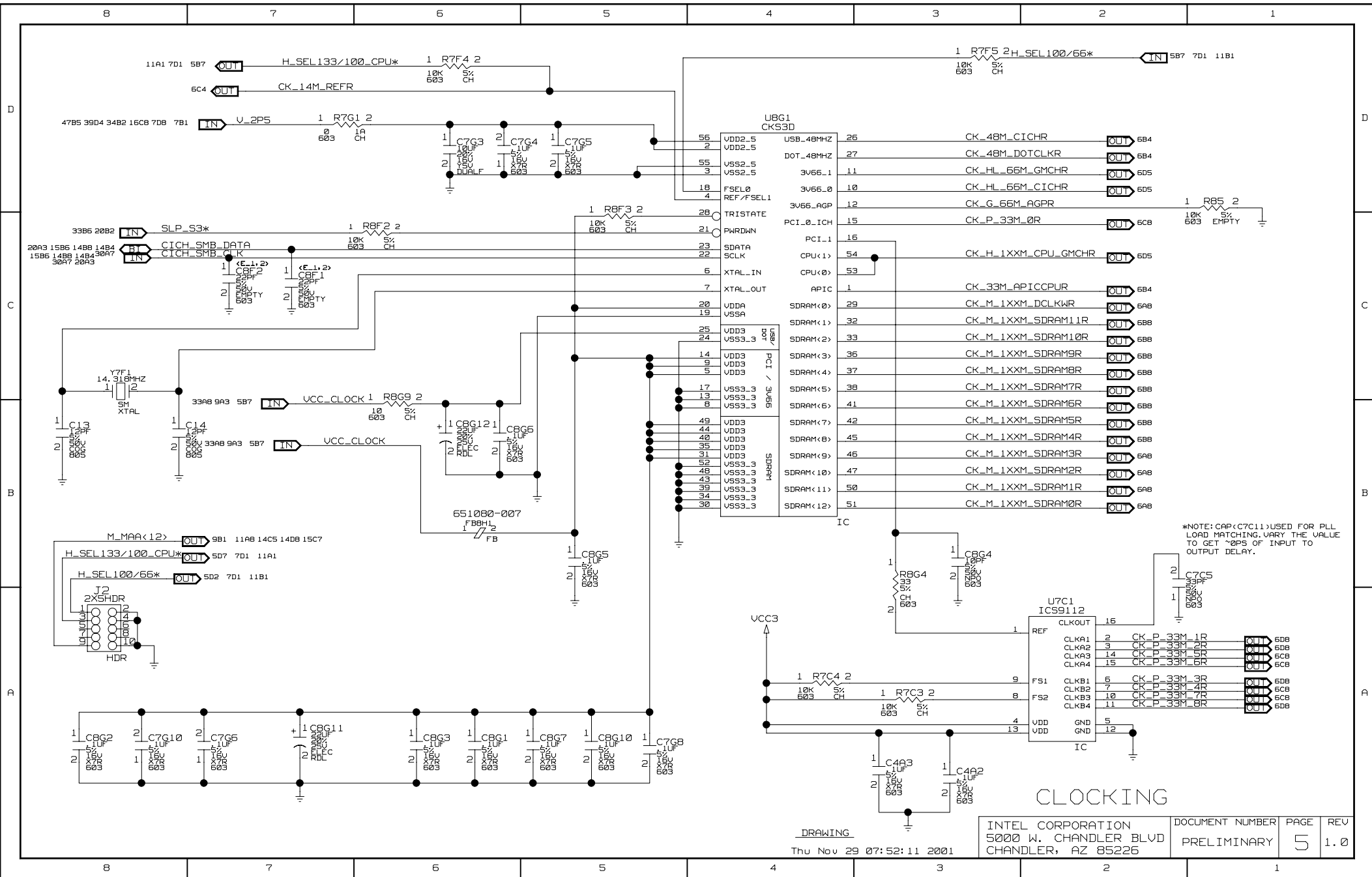
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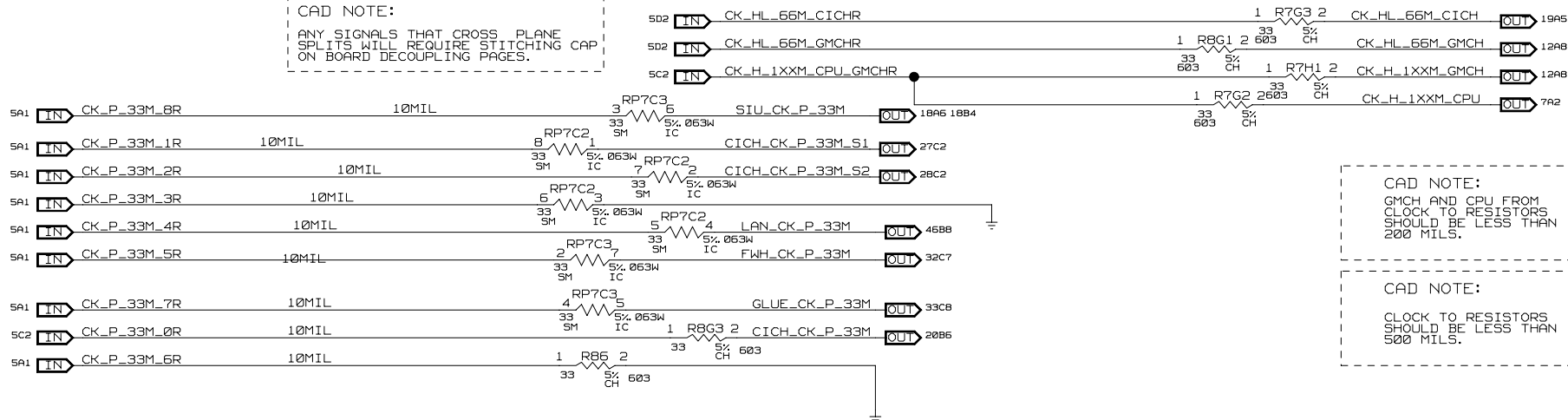
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ANY SIGNALS THAT CROSS PLANE  
SPLITS WILL REQUIRE STITCHING CAP  
ON BOARD DECOUPLING PAGES.

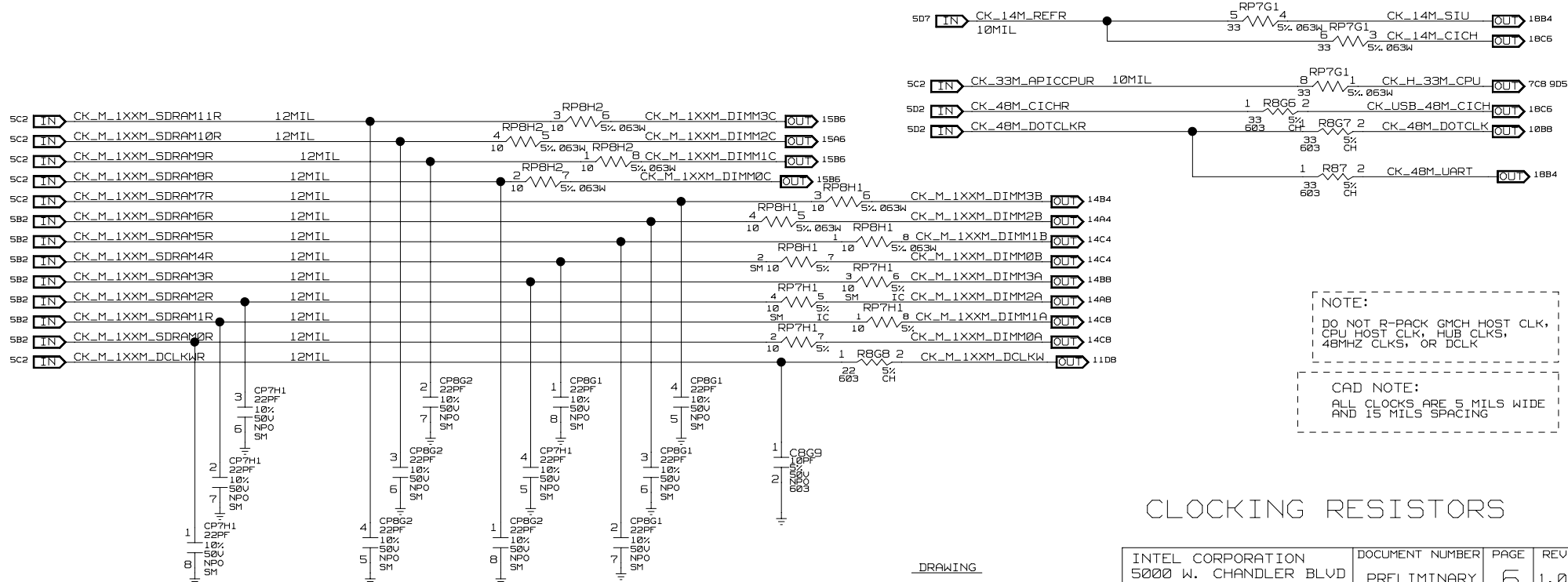


CAD NOTE:

GMCH AND CPU FROM  
CLOCK TO RESISTORS  
SHOULD BE LESS THAN  
200 MILS.

CAD NOTE:

CLOCK TO RESISTORS  
SHOULD BE LESS THAN  
500 MTL S.



NOTE:

DO NOT R-PACK GMCH HOST CLK,  
CPU HOST CLK, HUB CLKS,  
48MHZ CLKS, OR DCLK

CAD NOTE:

ALL CLOCKS ARE 5 MILS WIDE  
AND 15 MILS SPACING

## CLOCKING RESISTORS

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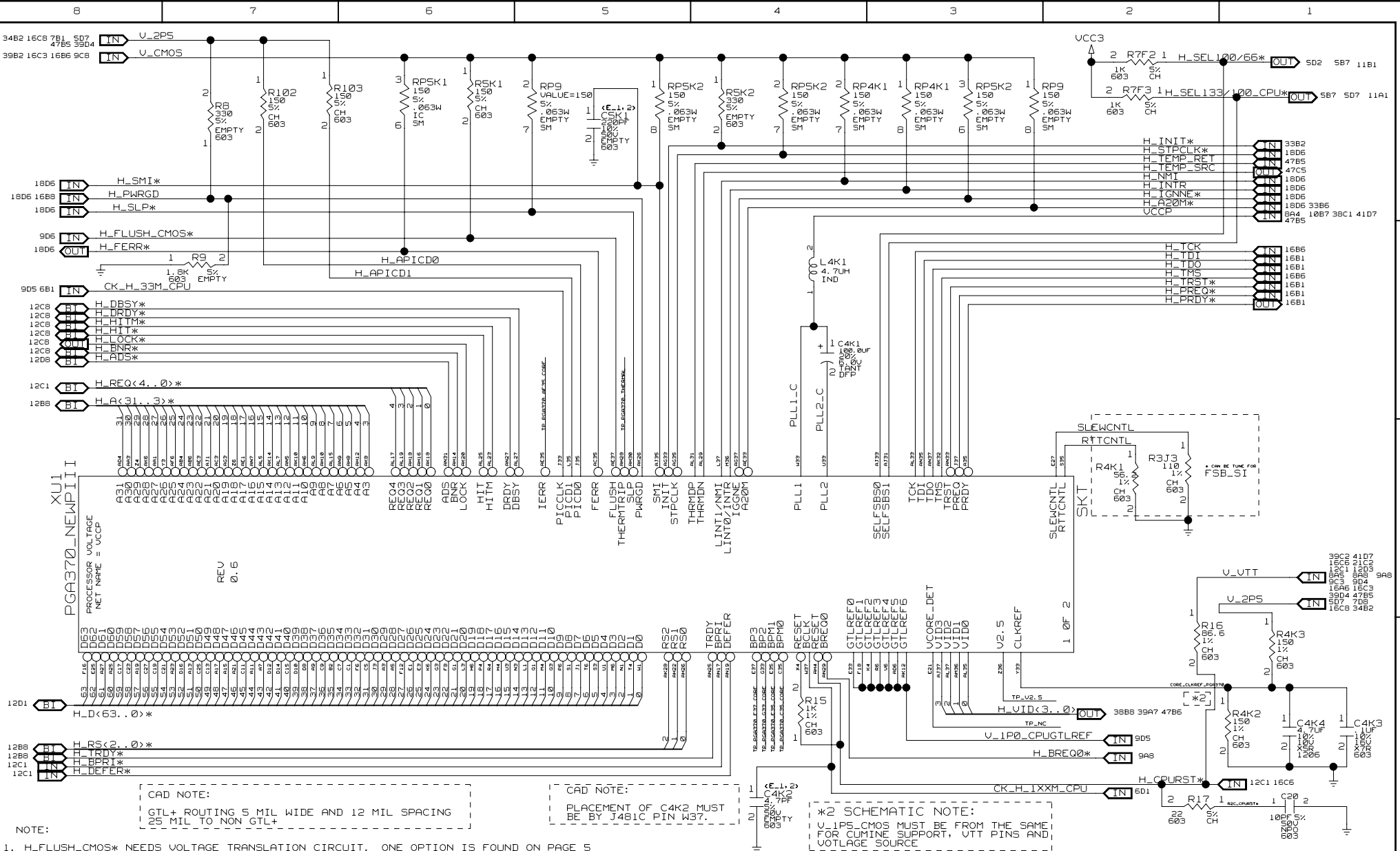
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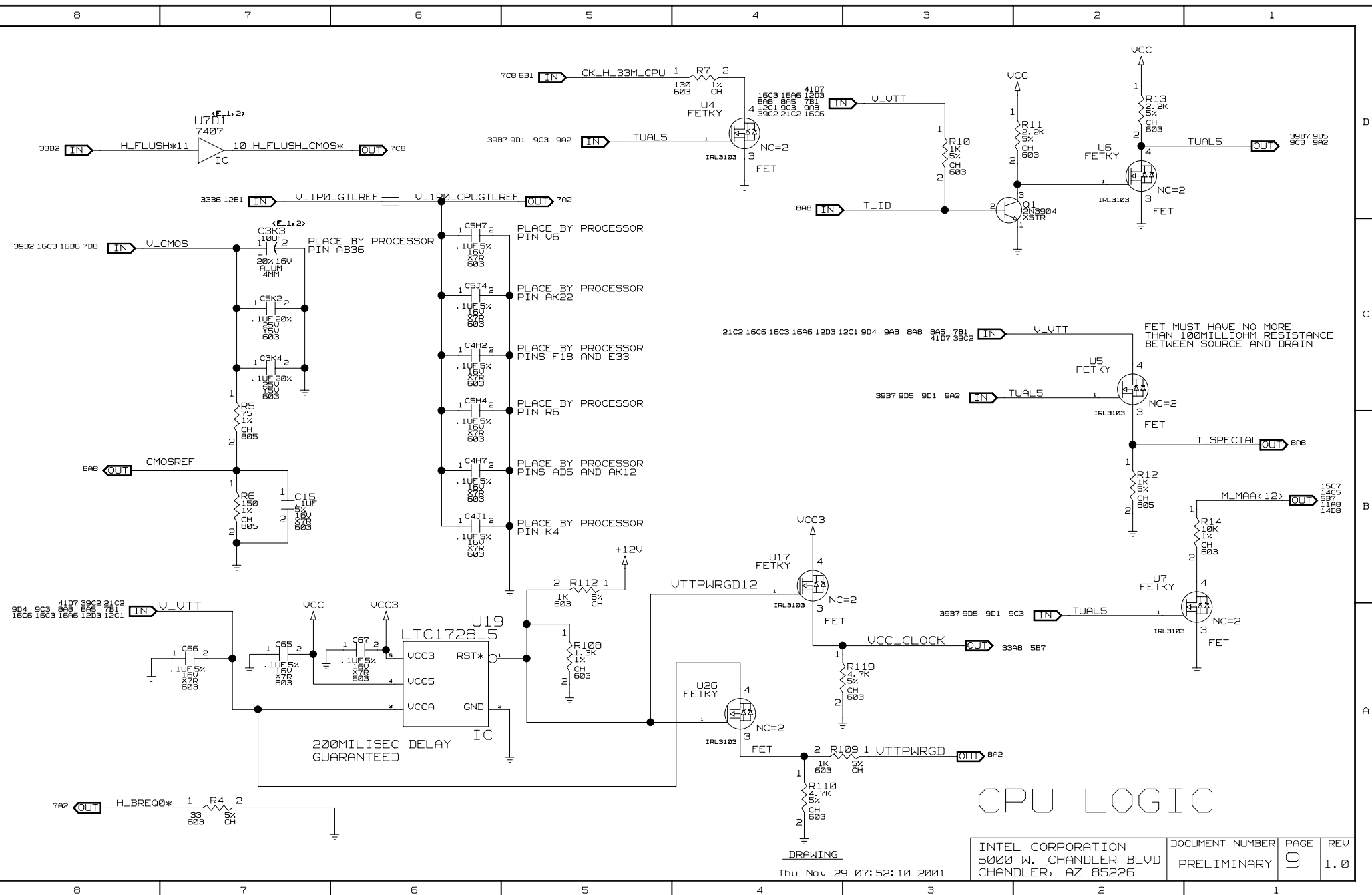
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CPU 1 OF 2 PGA370

CPU 2 OF 2 PGA370



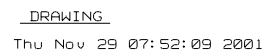


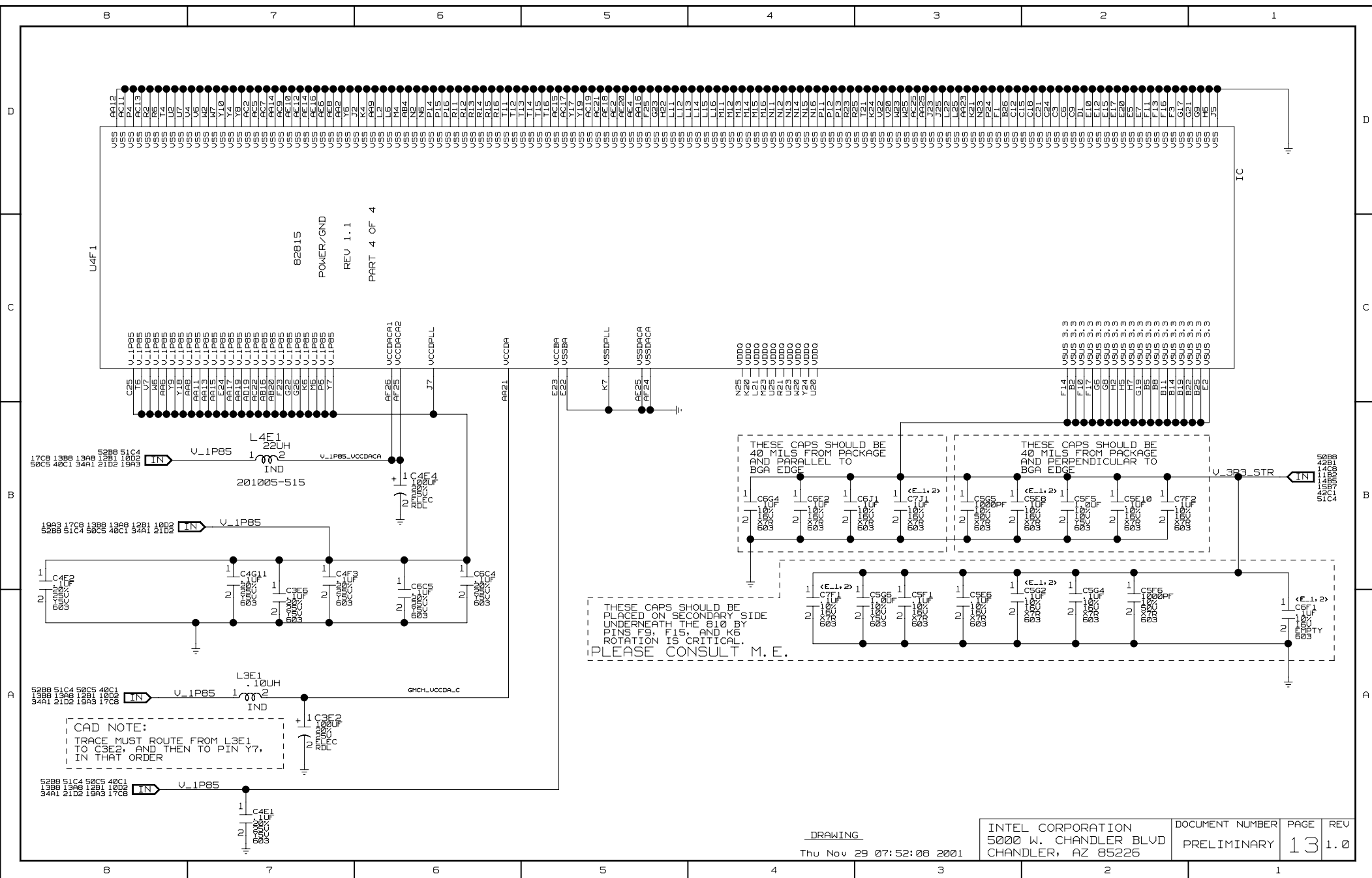


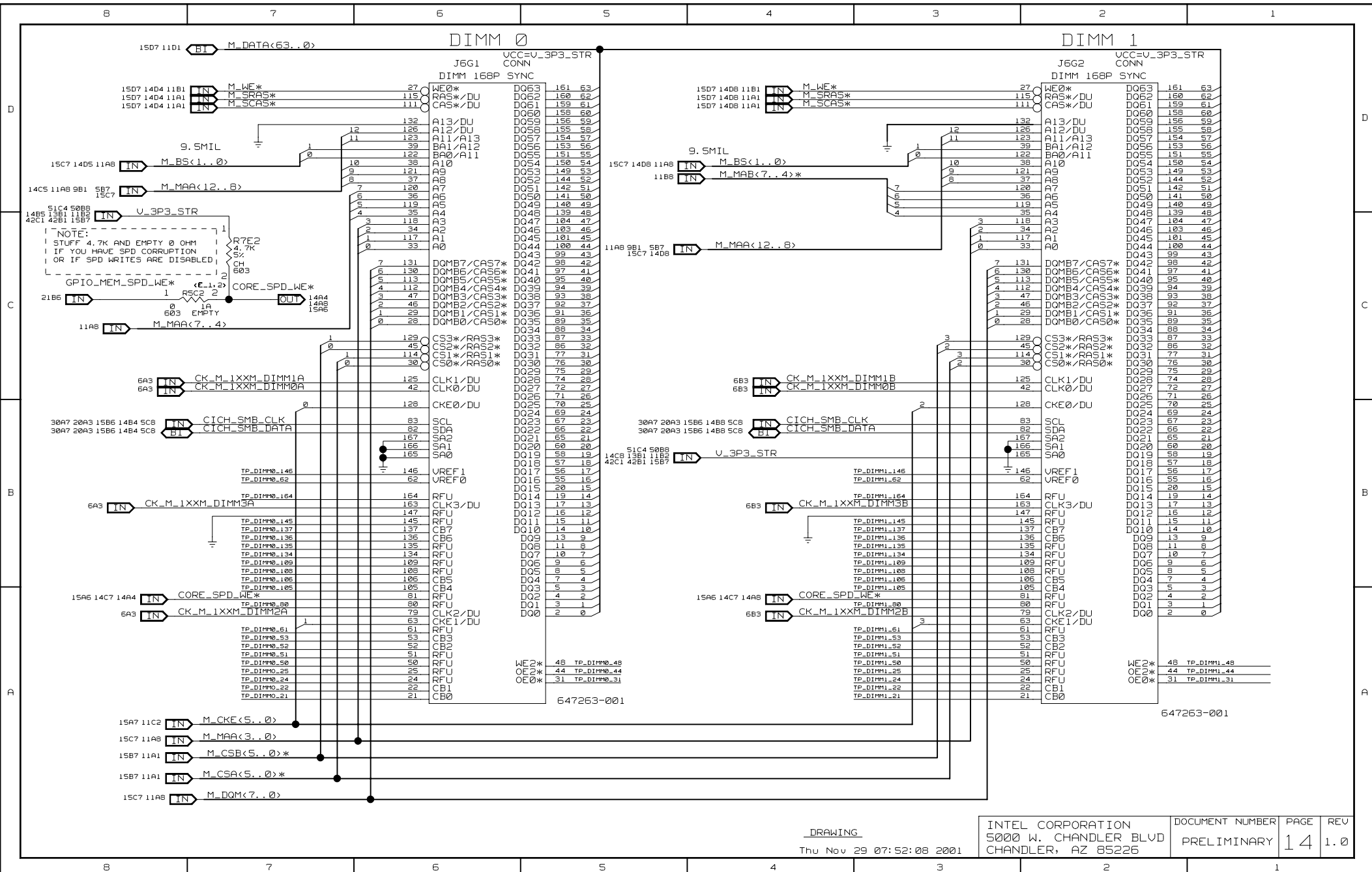
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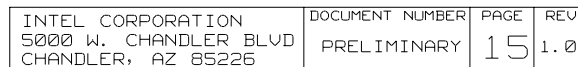
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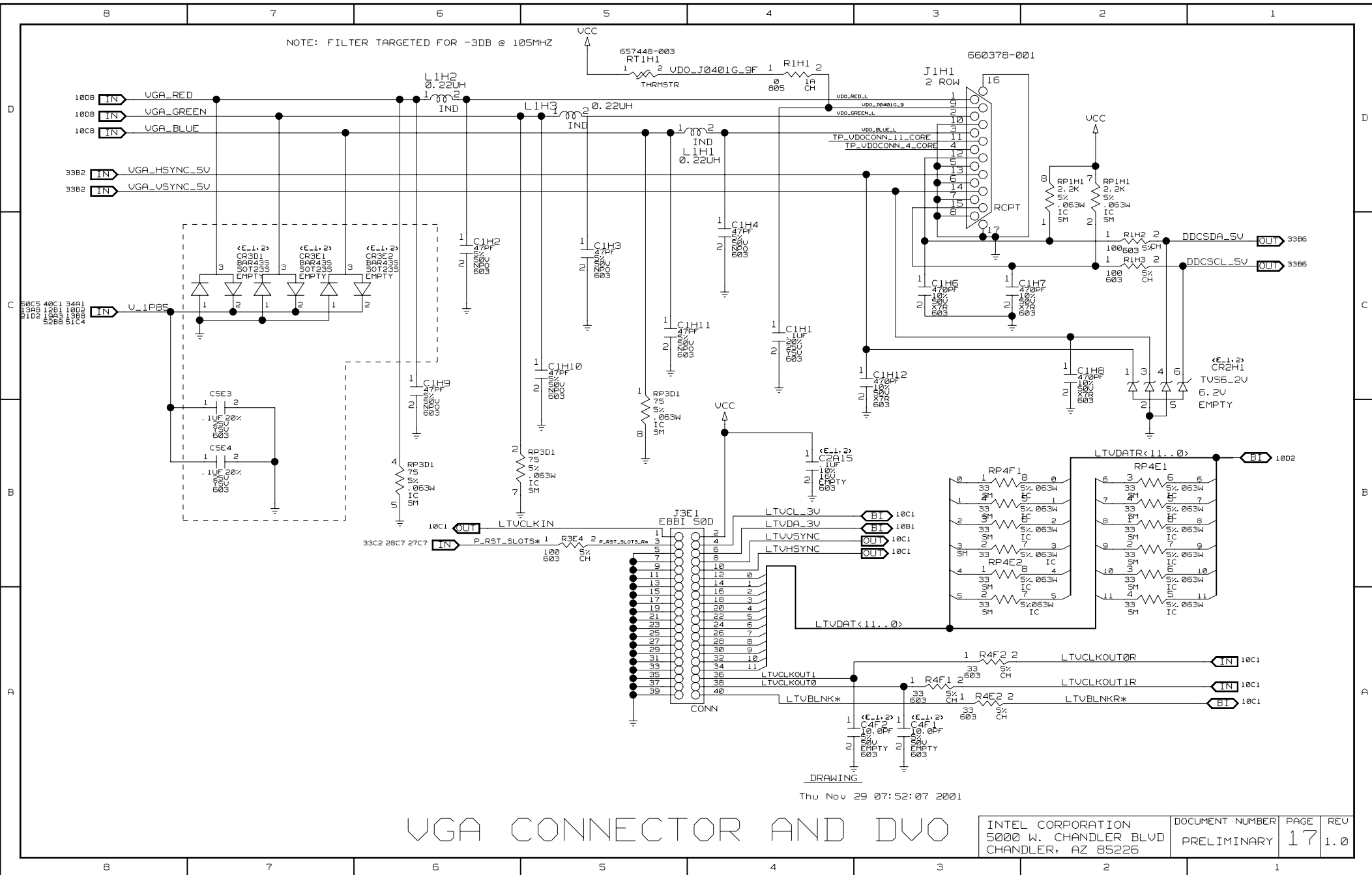


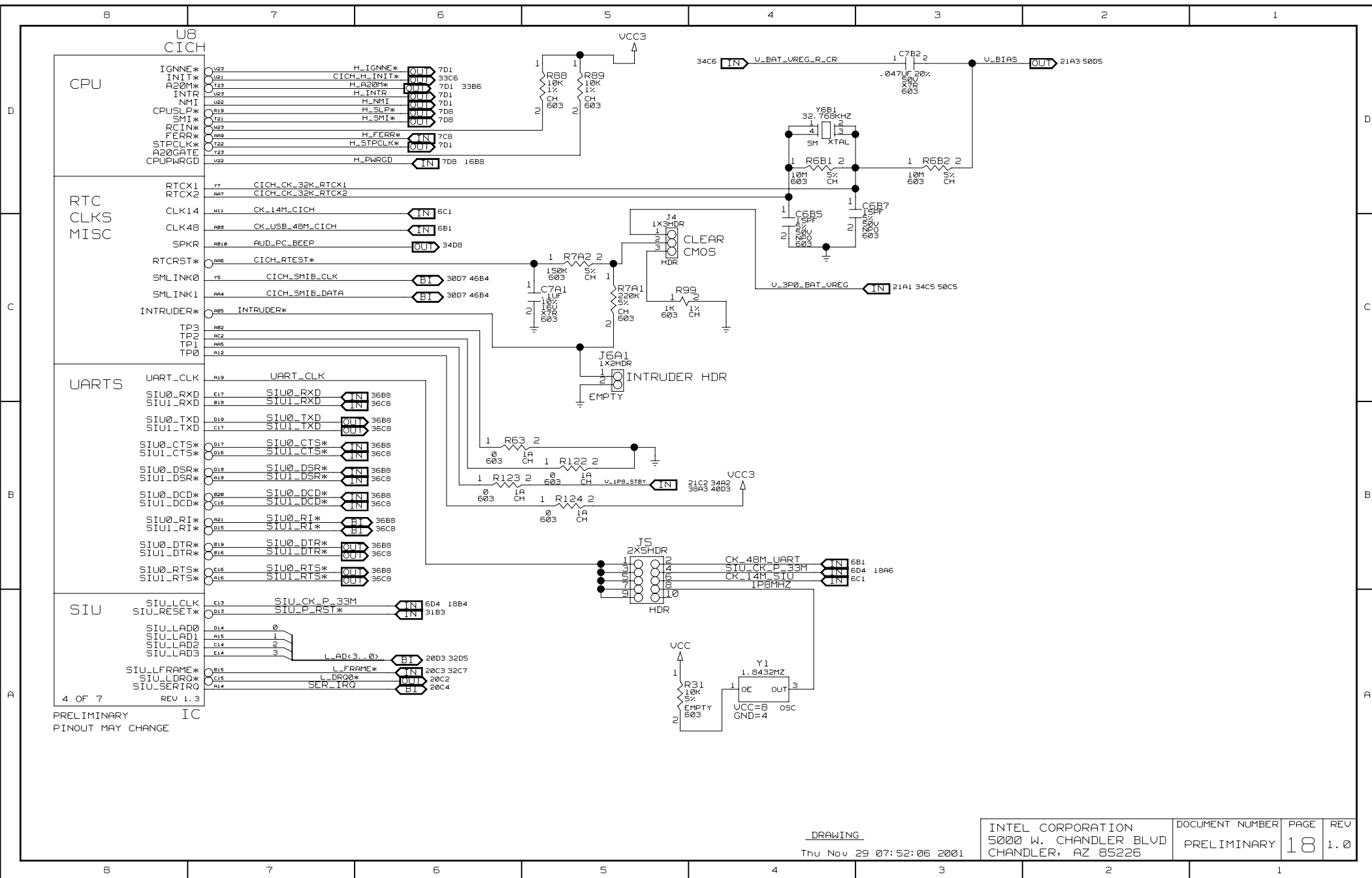










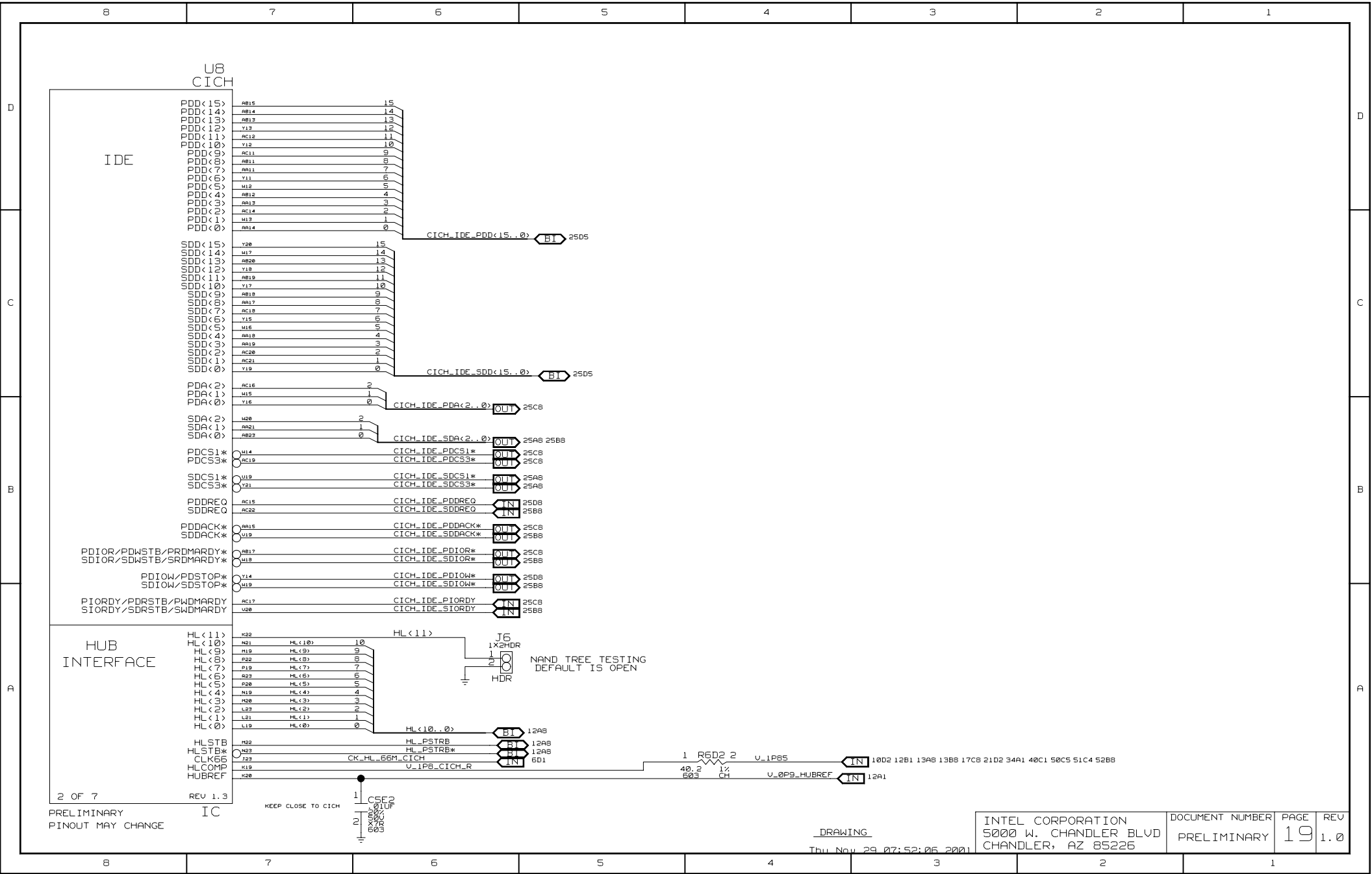


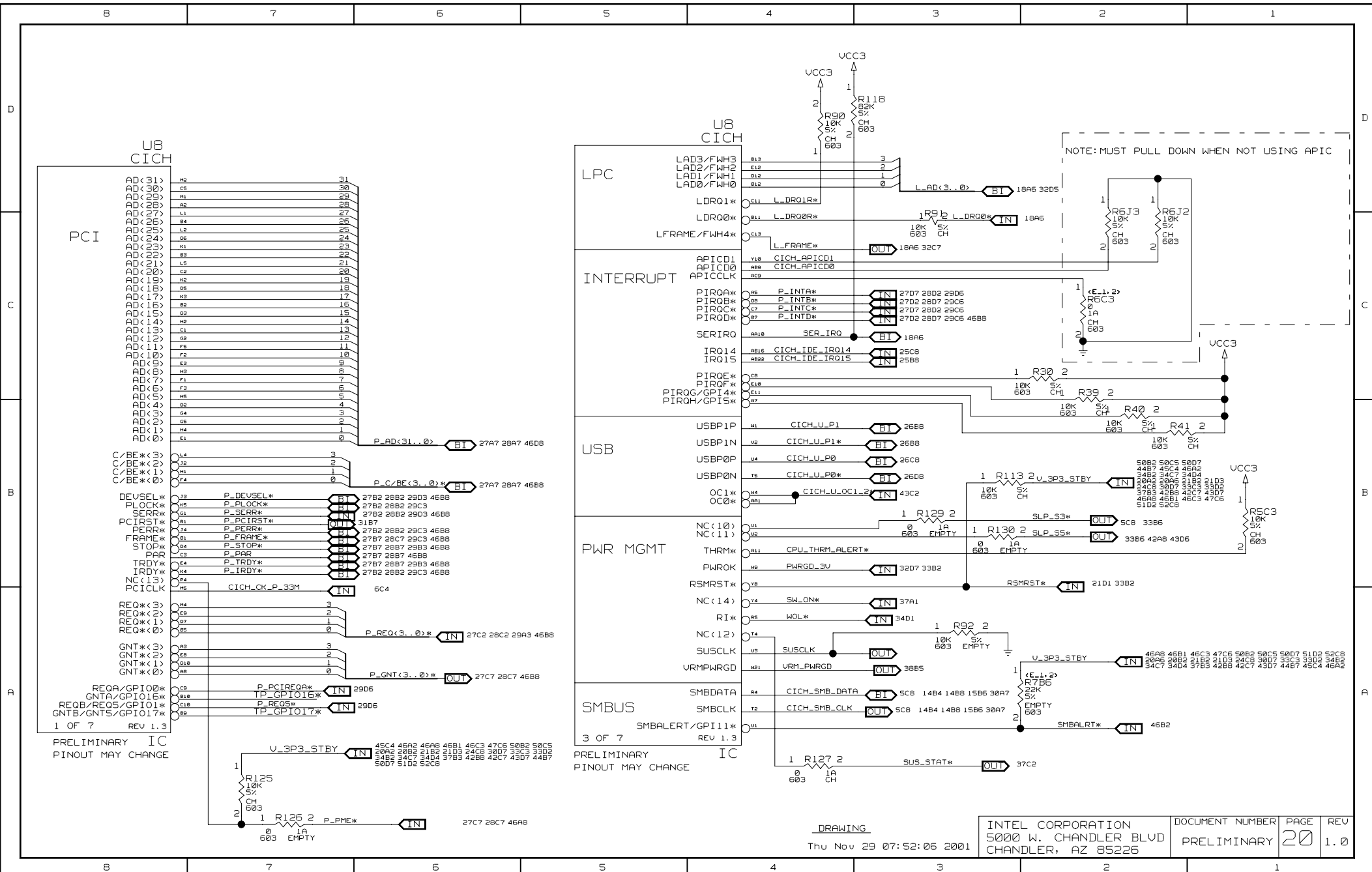
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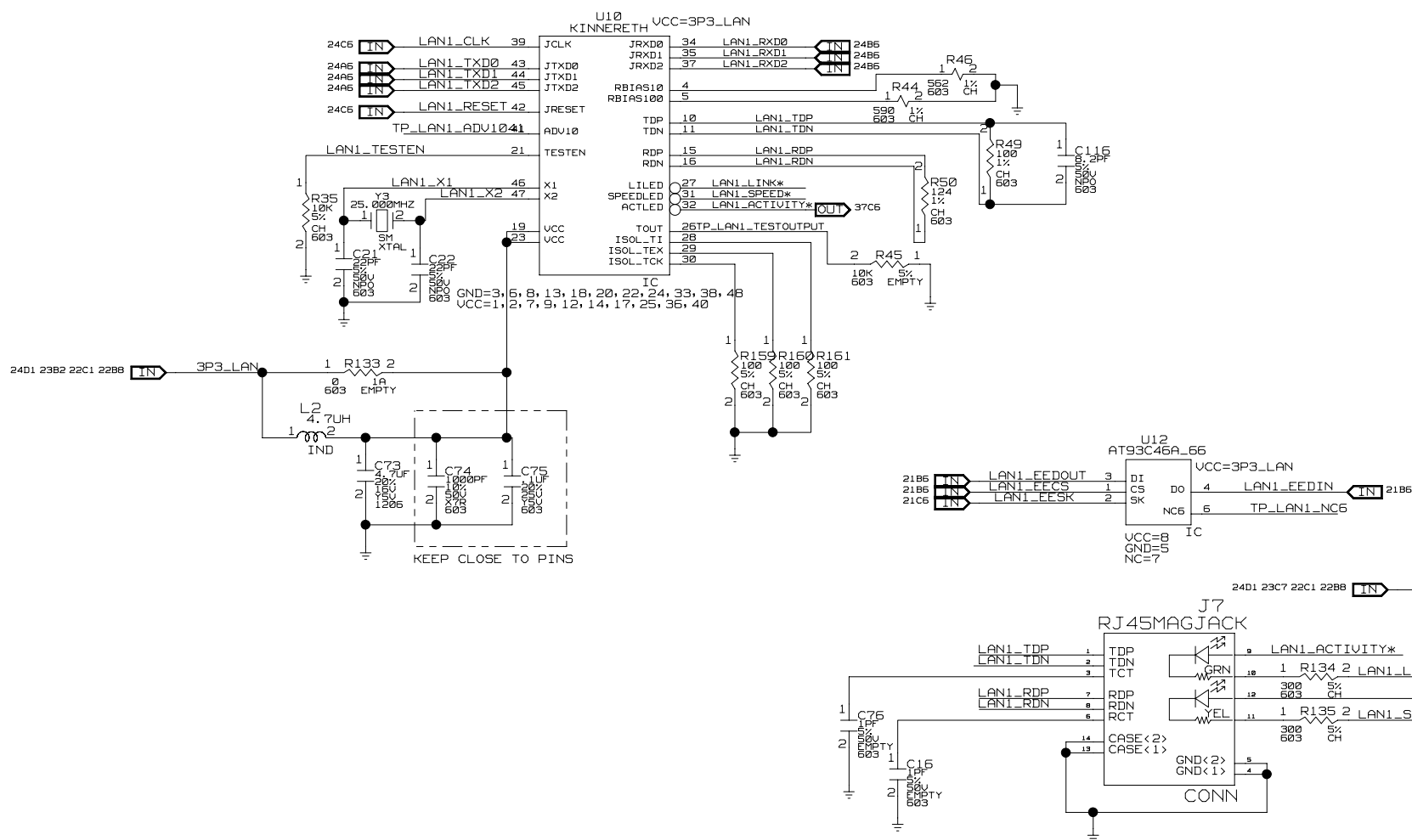


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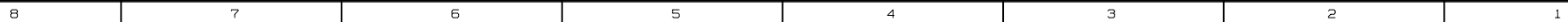


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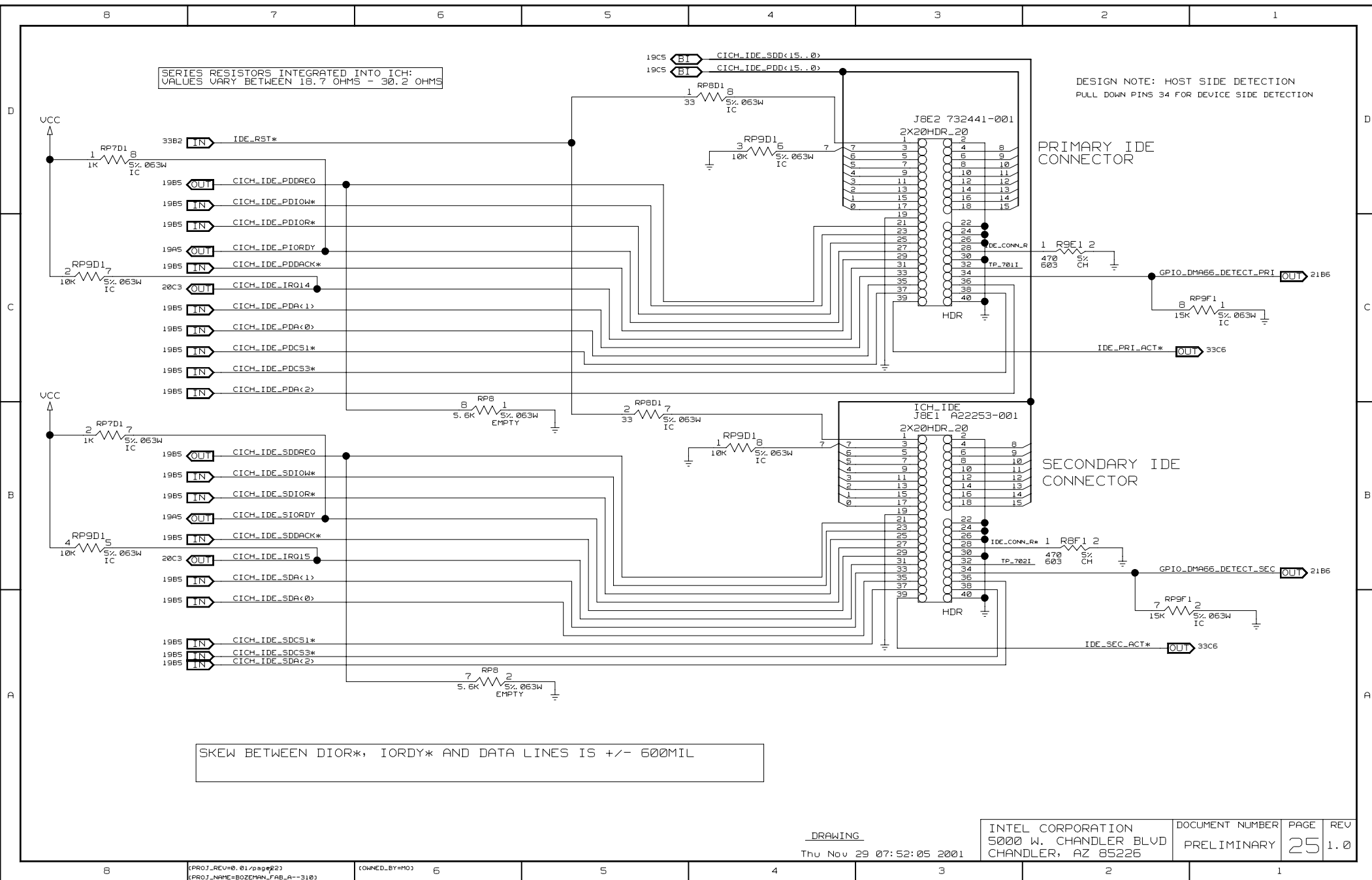
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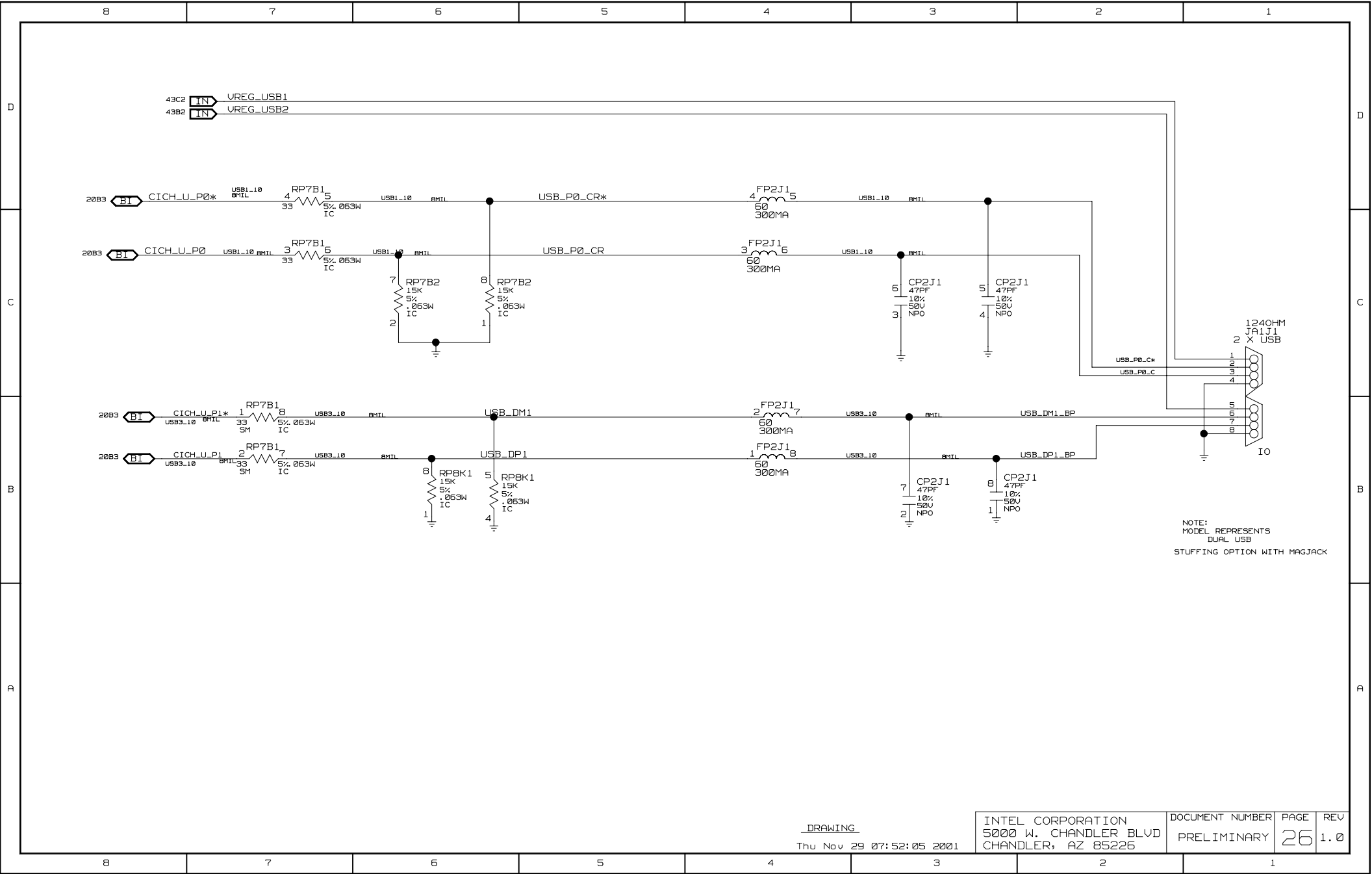
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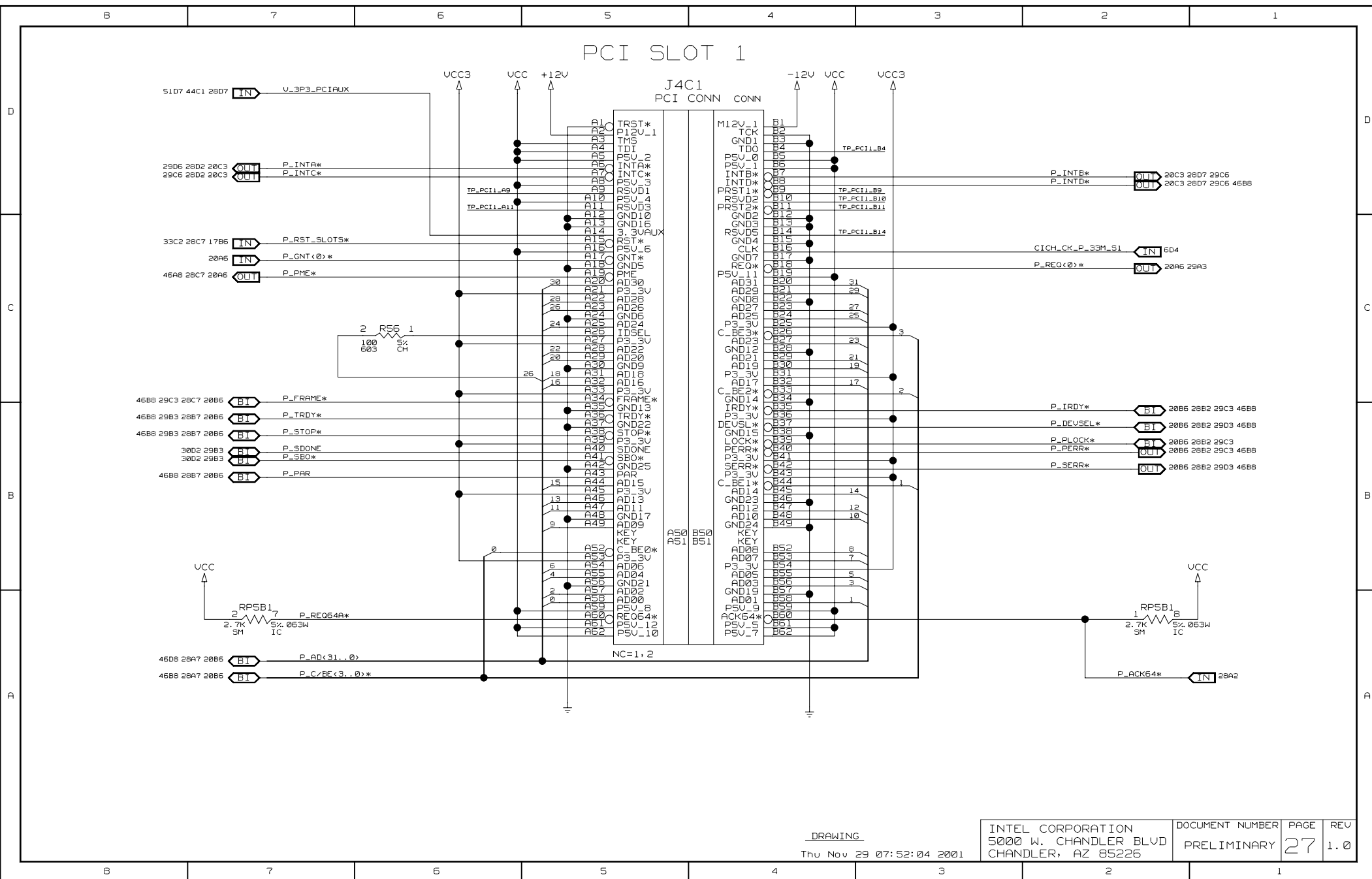
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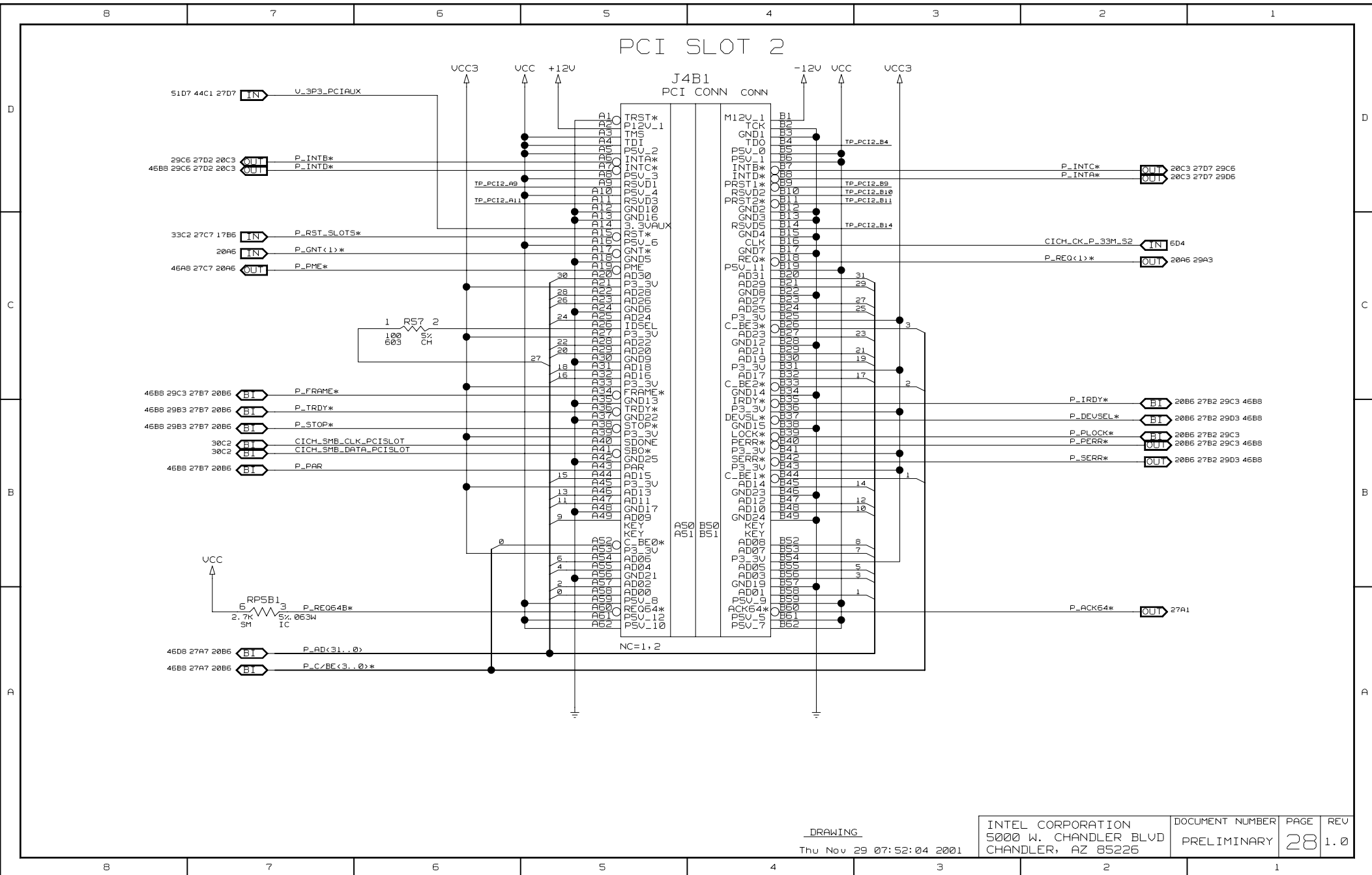
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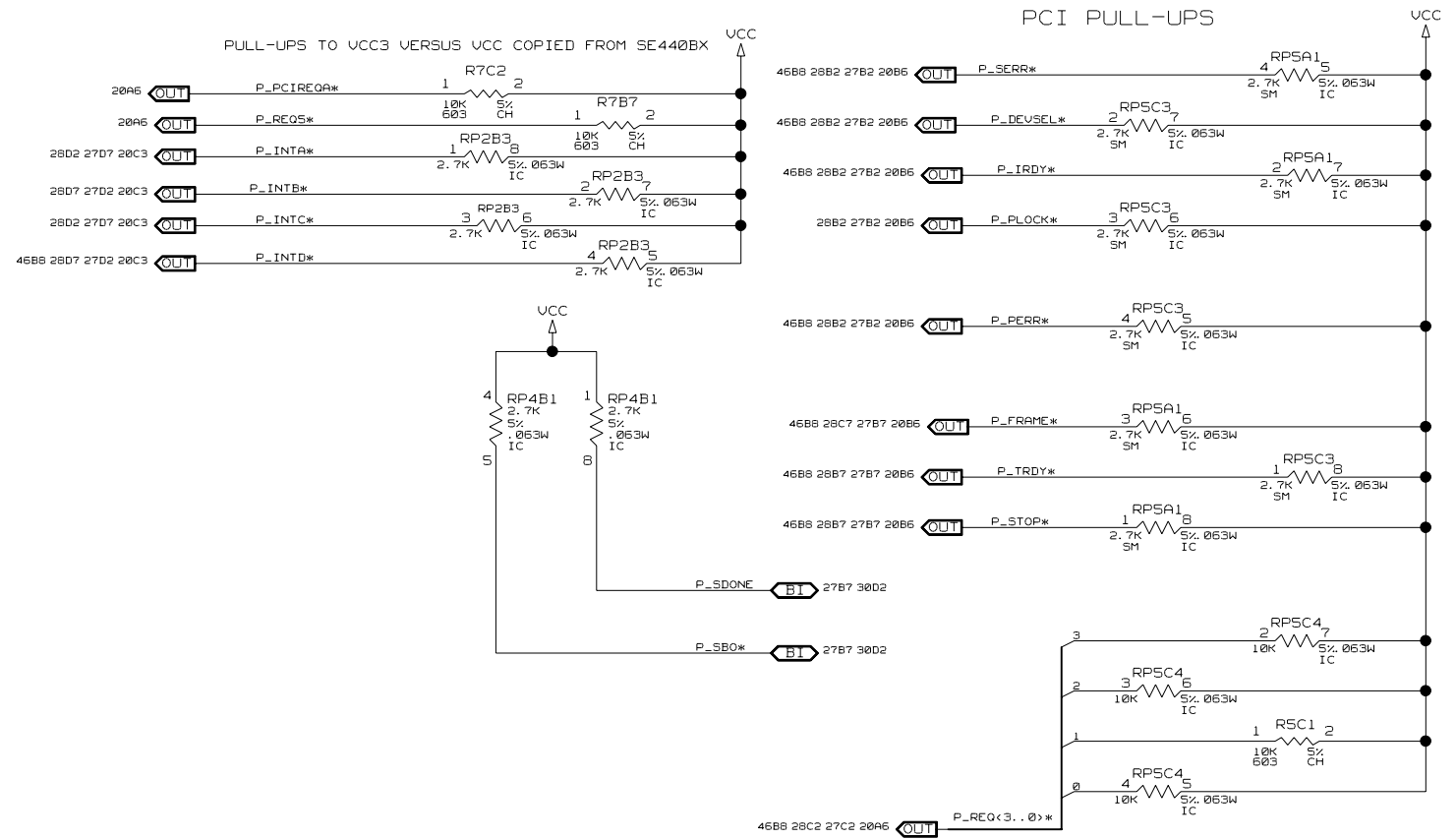
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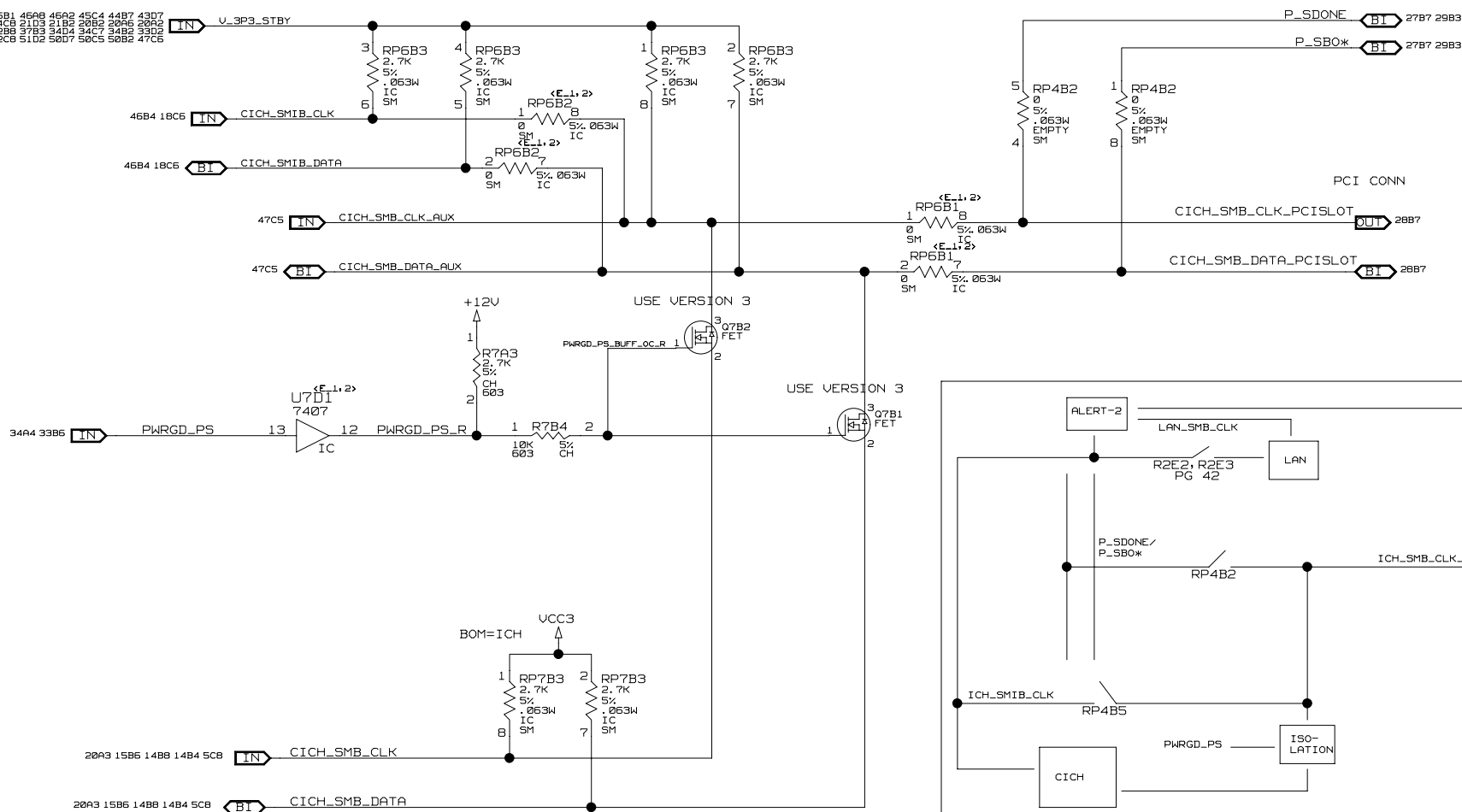
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39C3 24C8 21D3 21B2 20B2 20A6 20A2  
42C7 42B8 37B3 34D4 34C7 34B2 33D2  
52C8 51D2 50D7 50C5 50B2 47C6



## SMBUS SUPPORT

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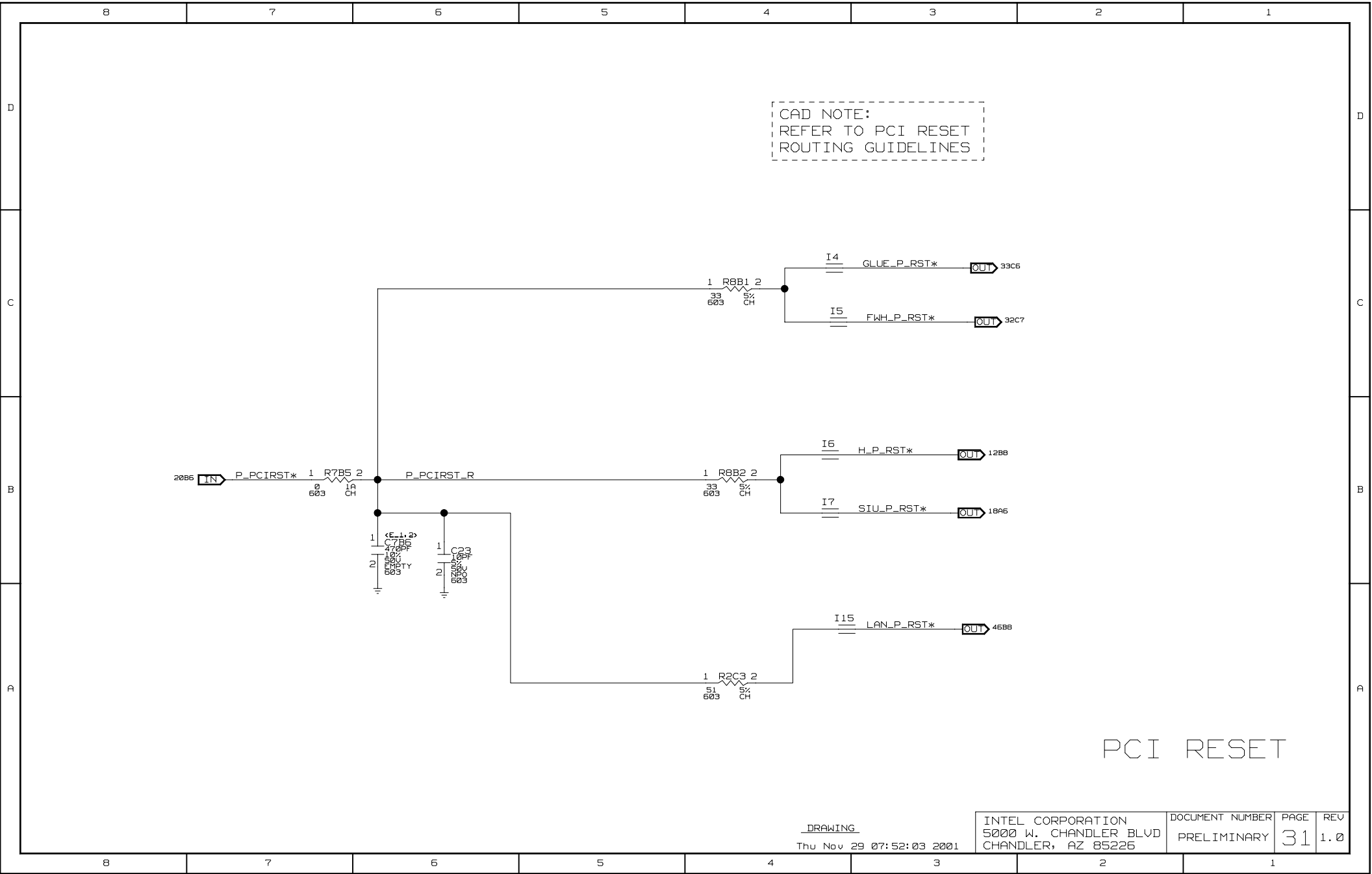
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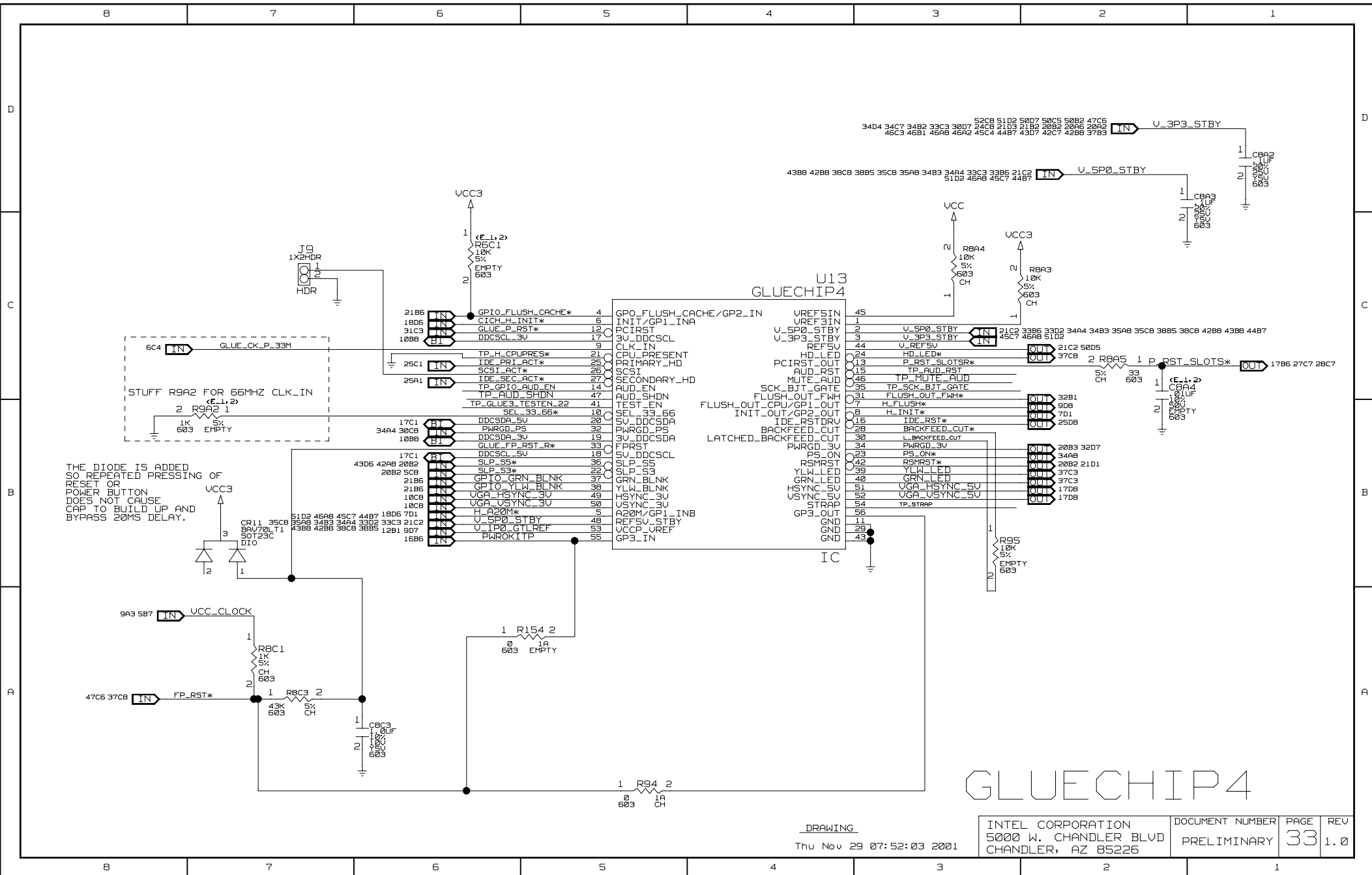


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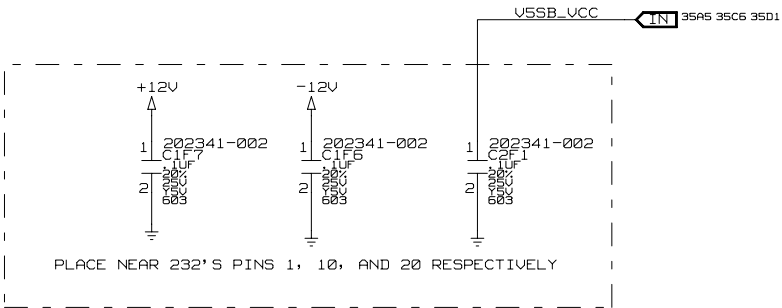
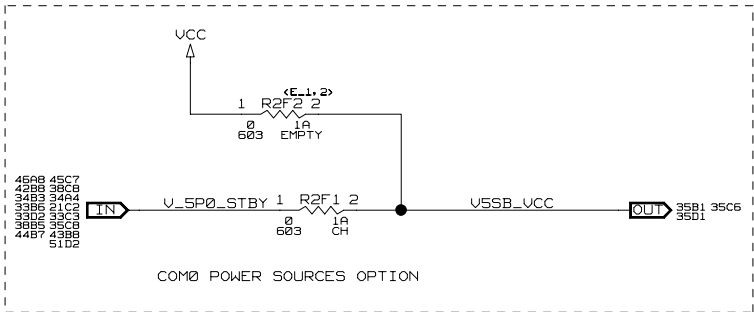
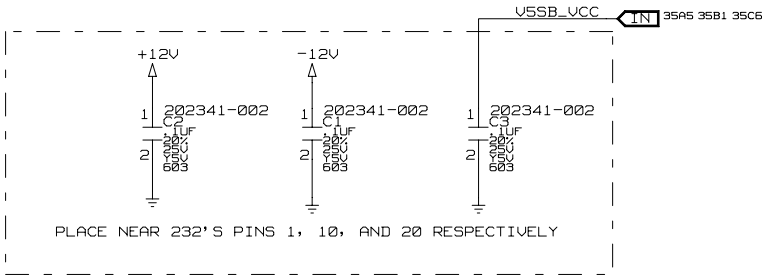
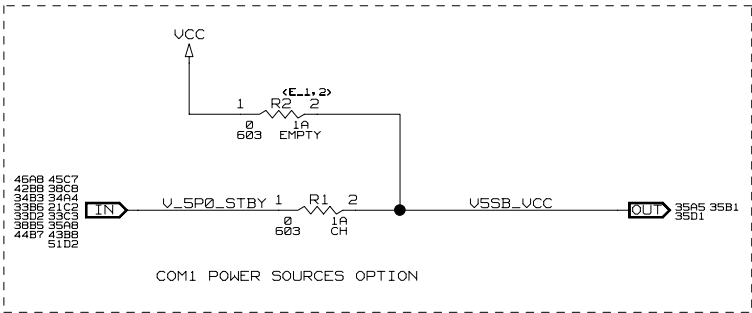








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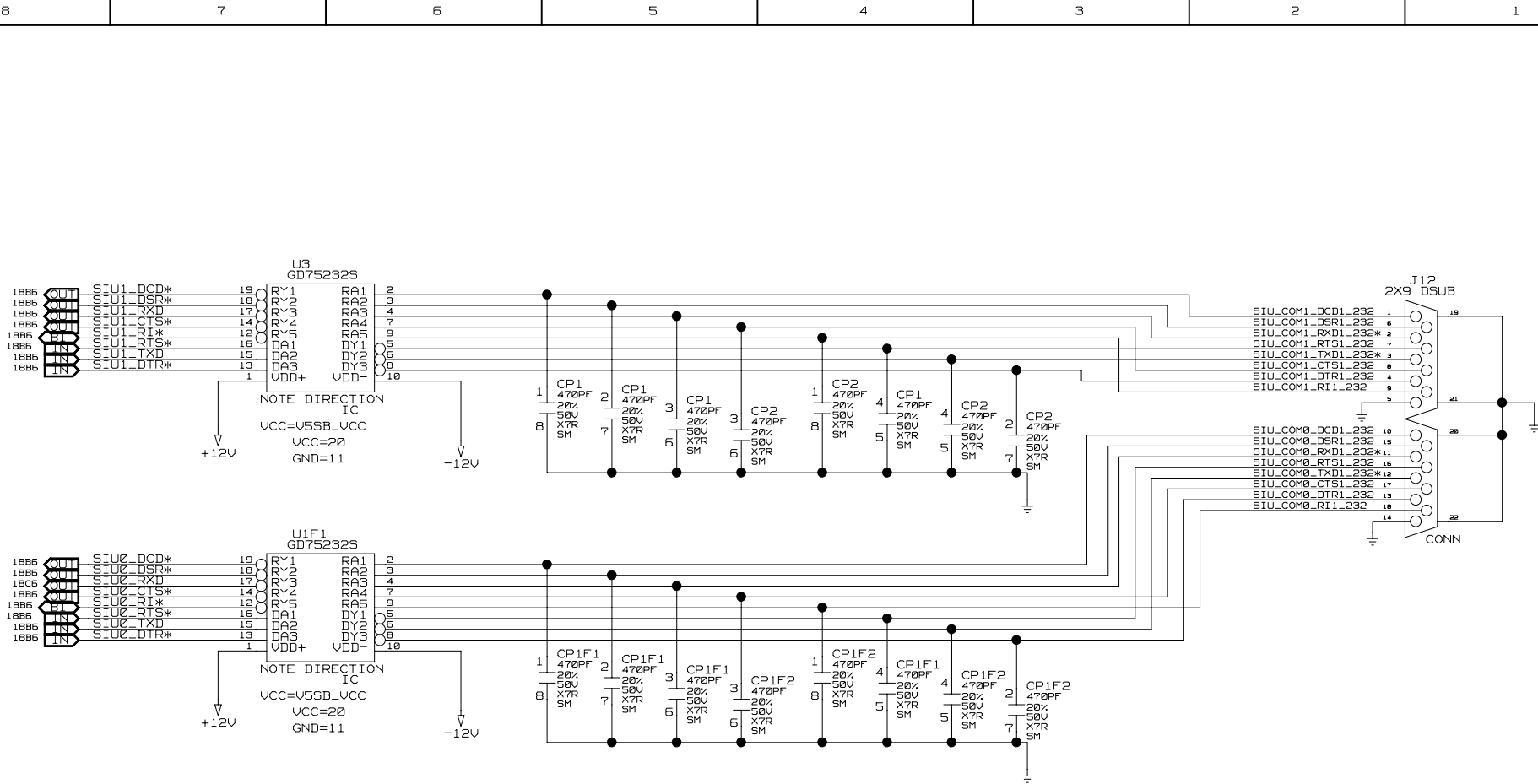


SERIAL INTERFACE PARTS

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## SERIAL INTERFACE

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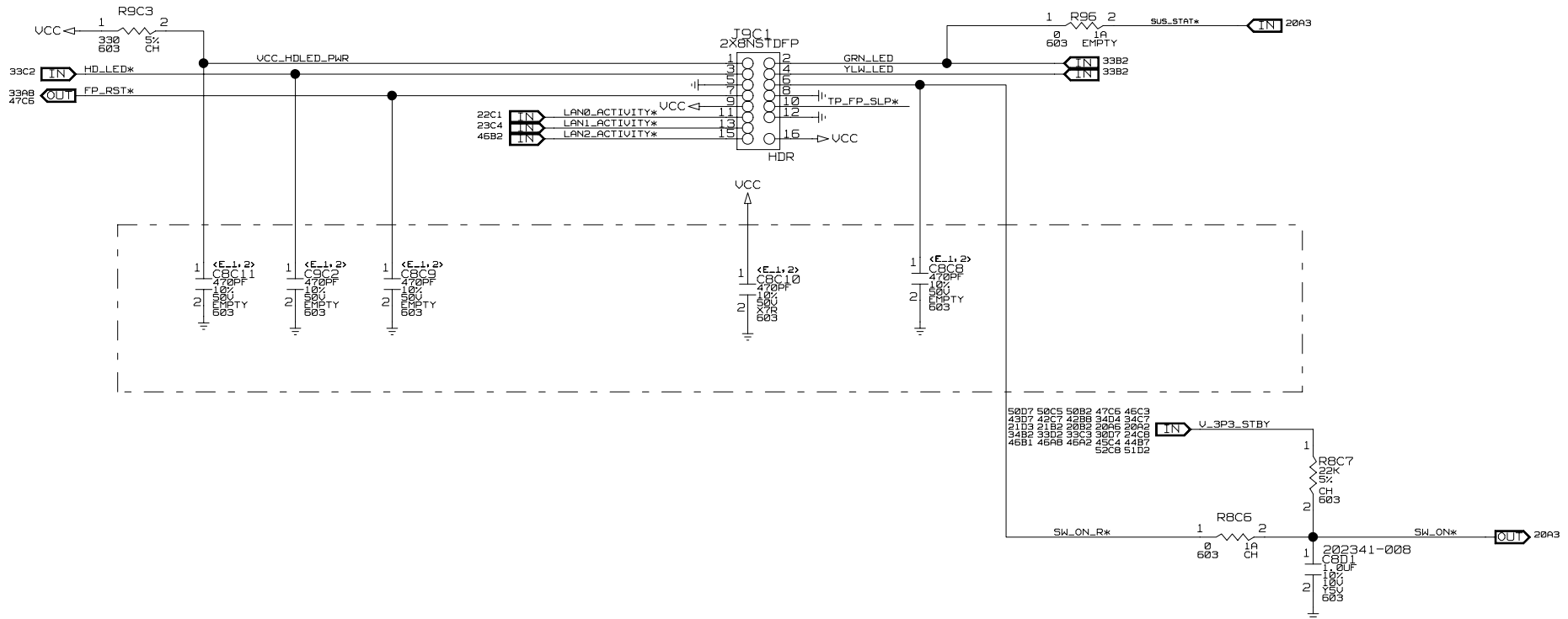
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LOC	LPC HDR	NO LPC HDR
R7C5	STUFFED	EMPTY
R7C6	EMPTY	STUFFED
R8D1	EMPTY	STUFFED
R7D3	STUFFED	EMPTY

ADD COMMENT NEXT TO SWITCH  
AS SILKSCREEN NEXT TO BUTTON.  
PLACE BUTTONS NEAR HEADER J9C1



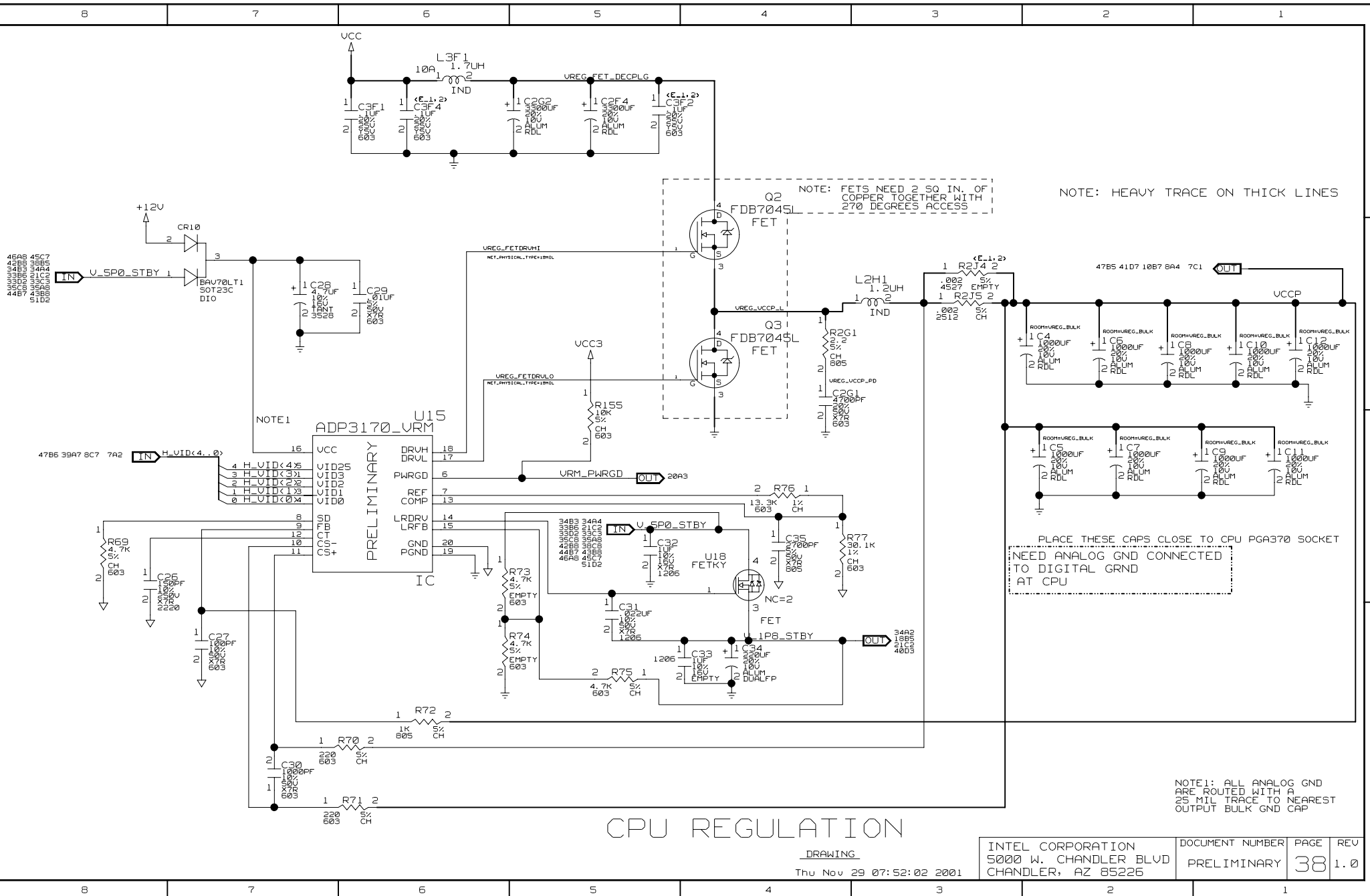
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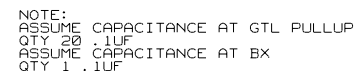
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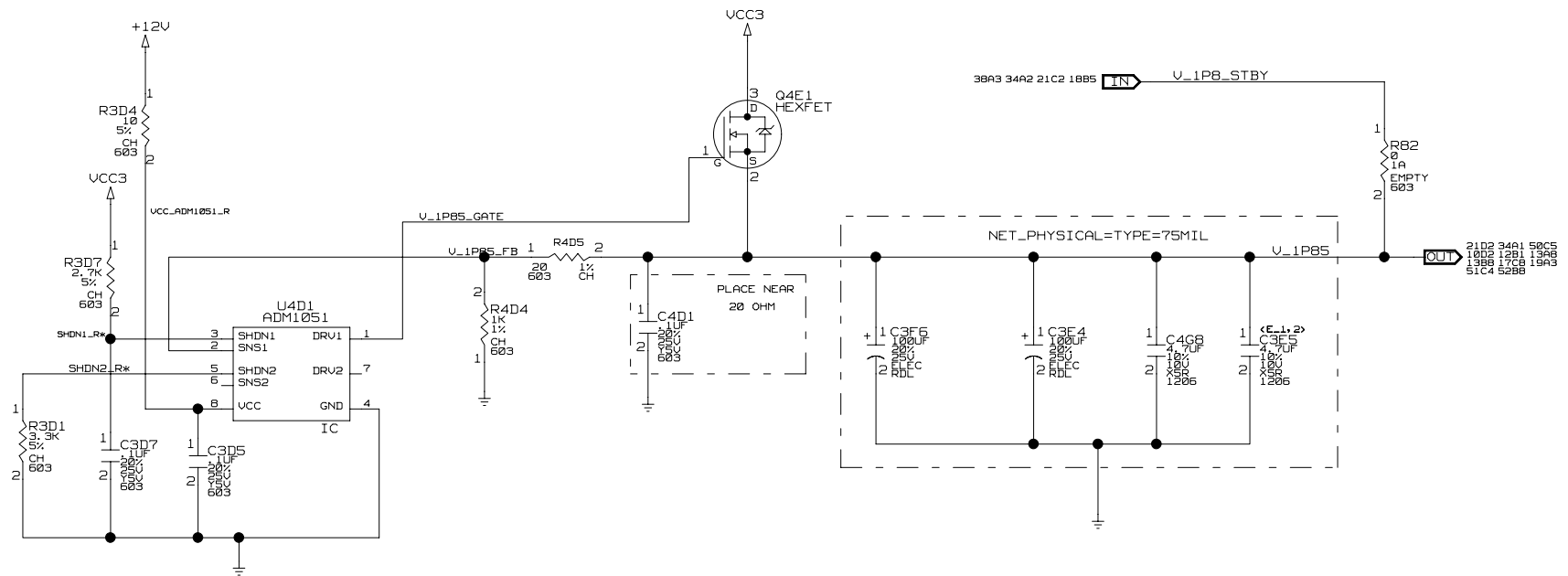
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# LINEAR REGULATOR

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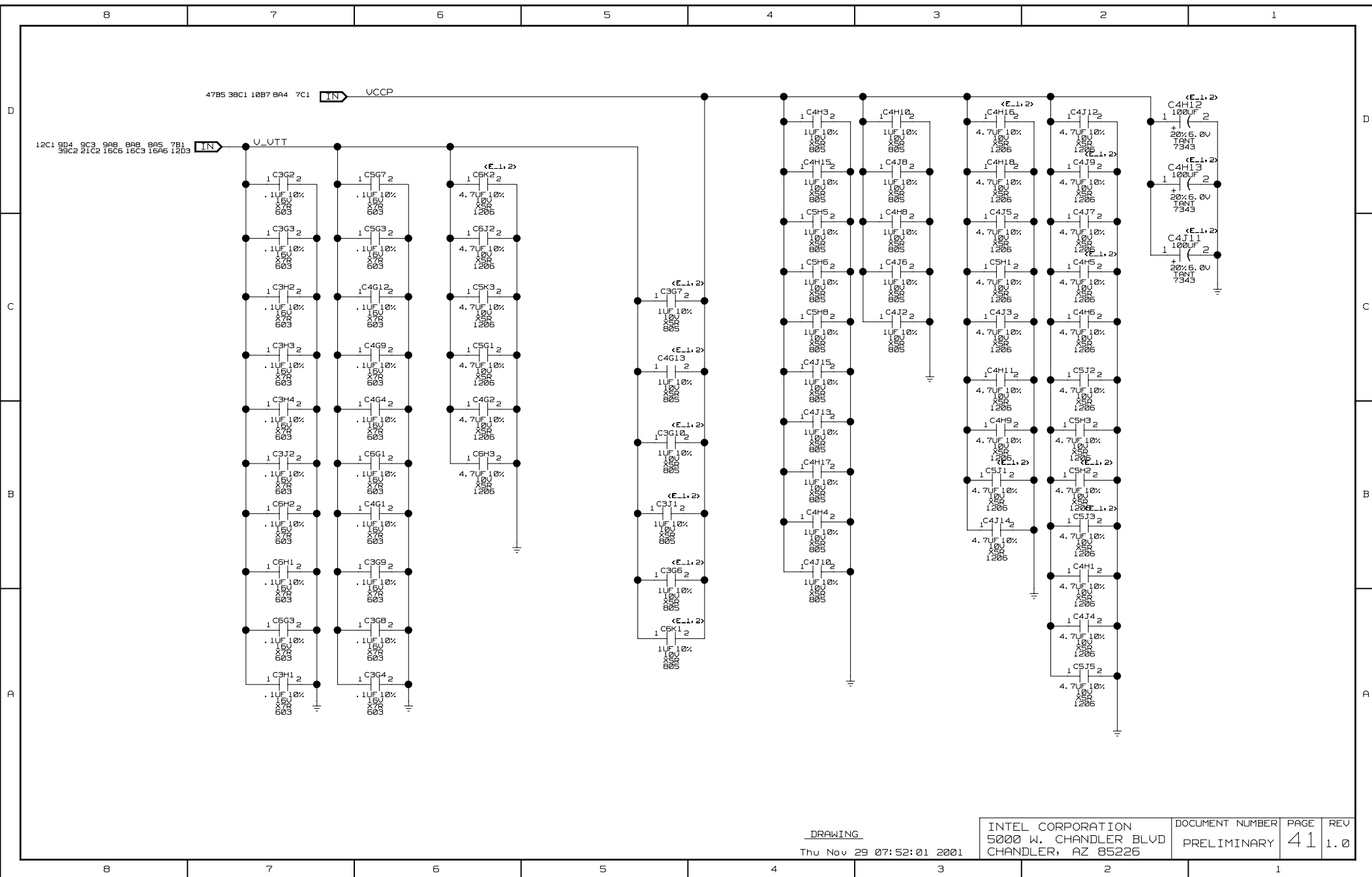
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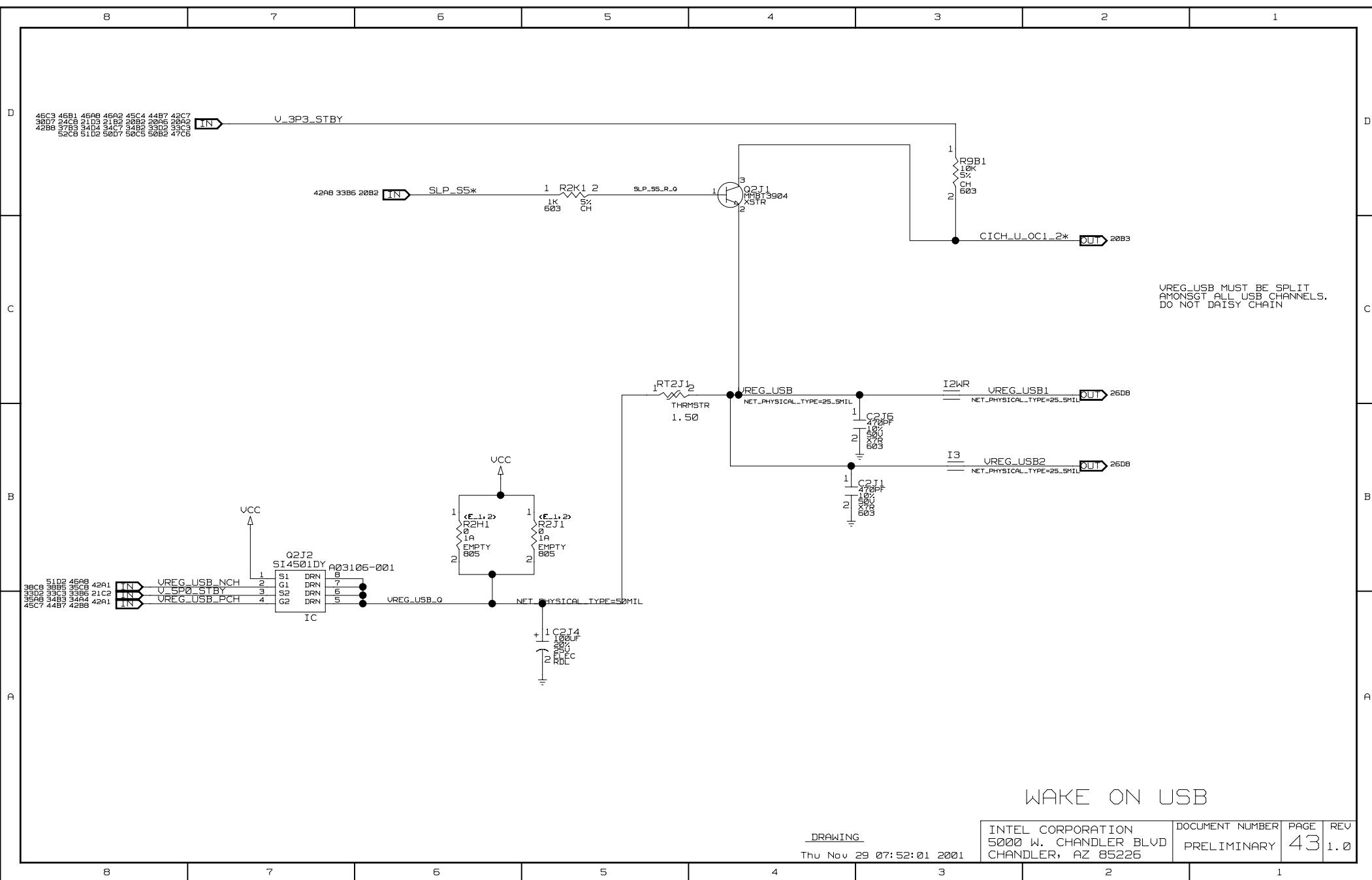


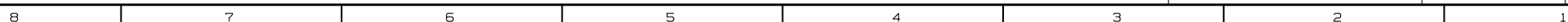




VREG_FEEDBACK1		VREG_USB_NCH	NTM4388
VREG_FEEDBACK2			

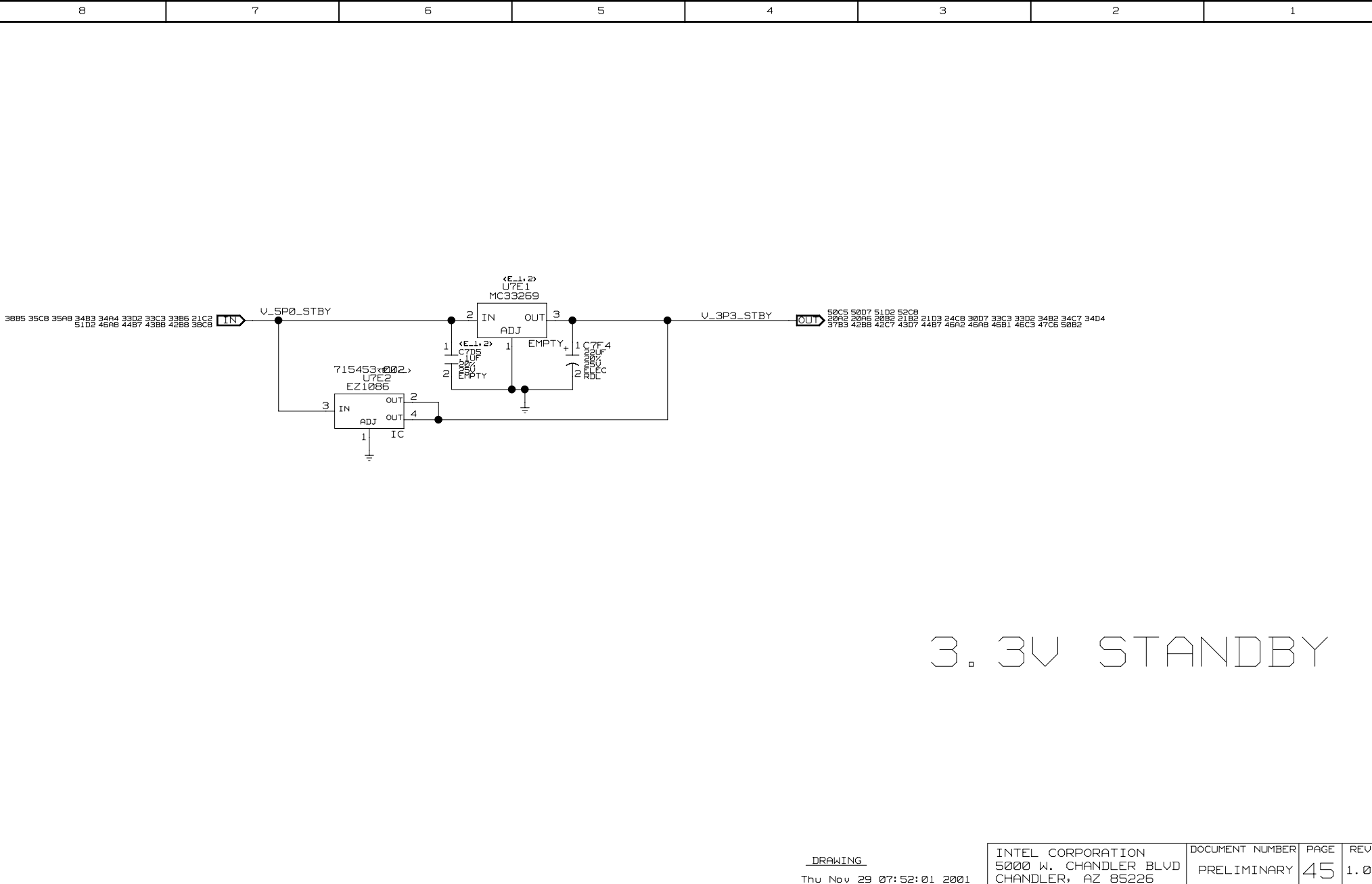
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3.3V STANDBY

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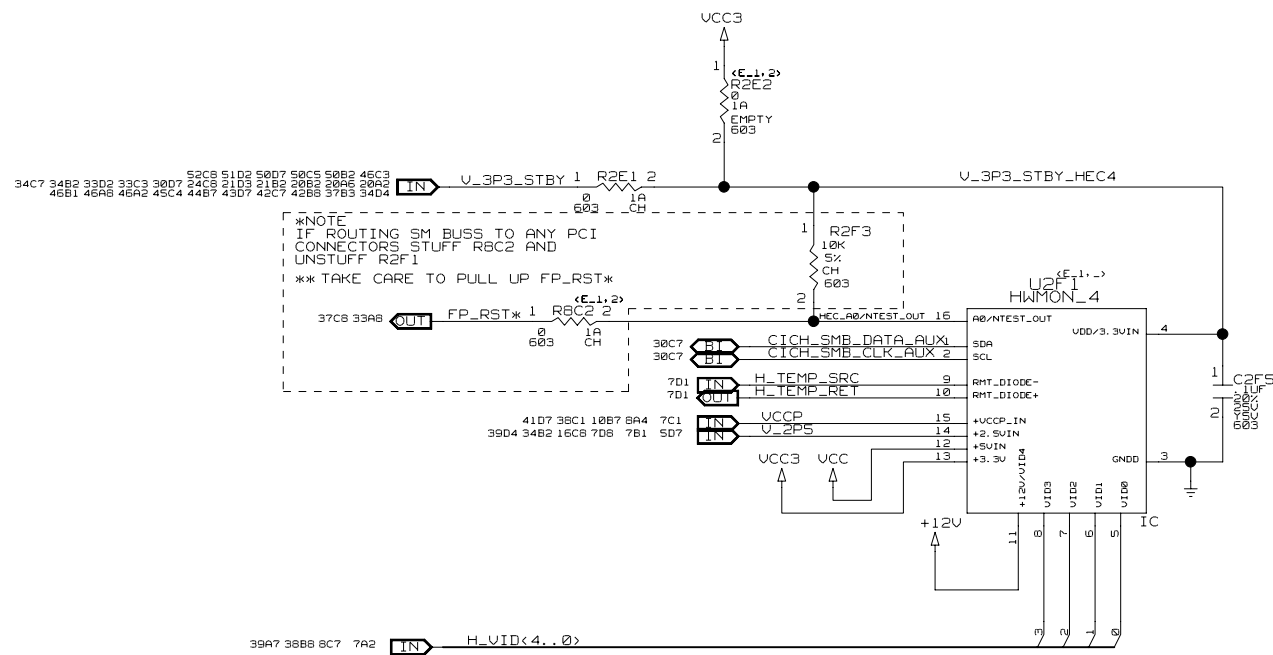
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WITH DUAL USB MAGJACK CONNECTOR

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## HARDWARE MONITOR 4

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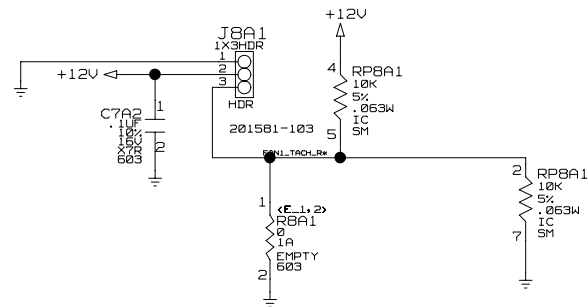
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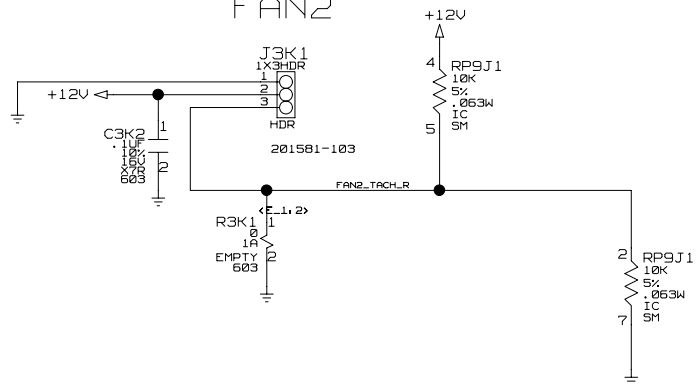
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## FAN1



## FAN2



## FAN CONTROL

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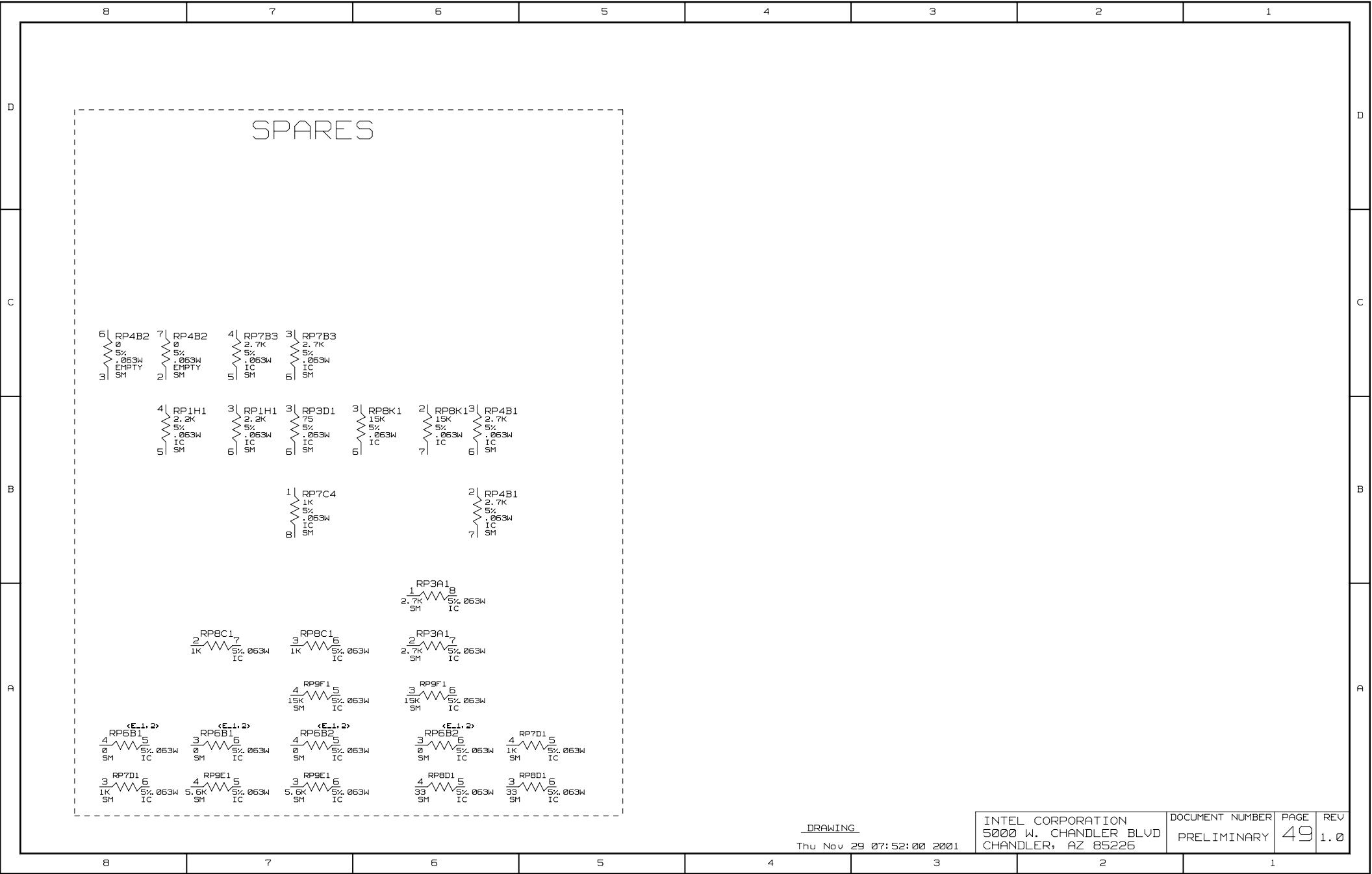
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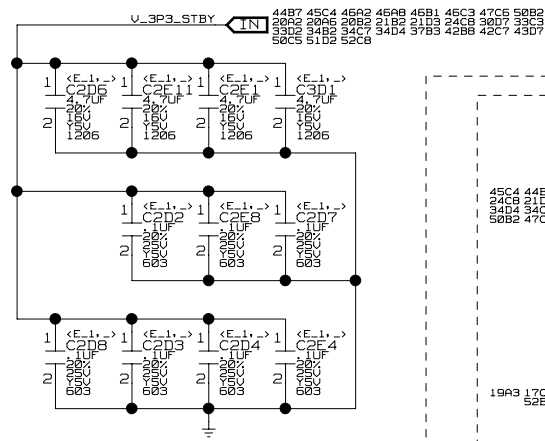
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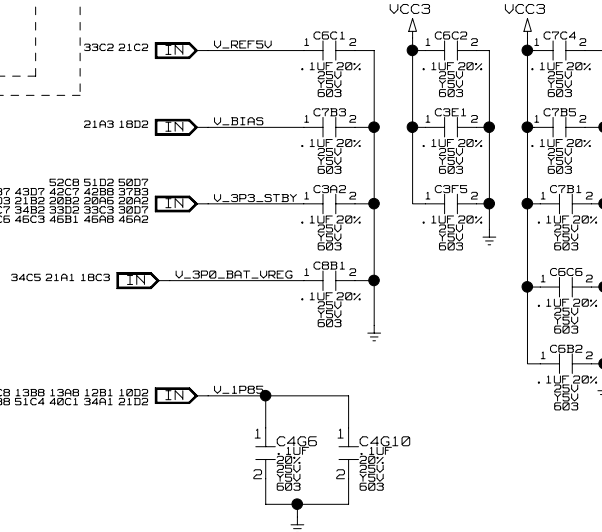
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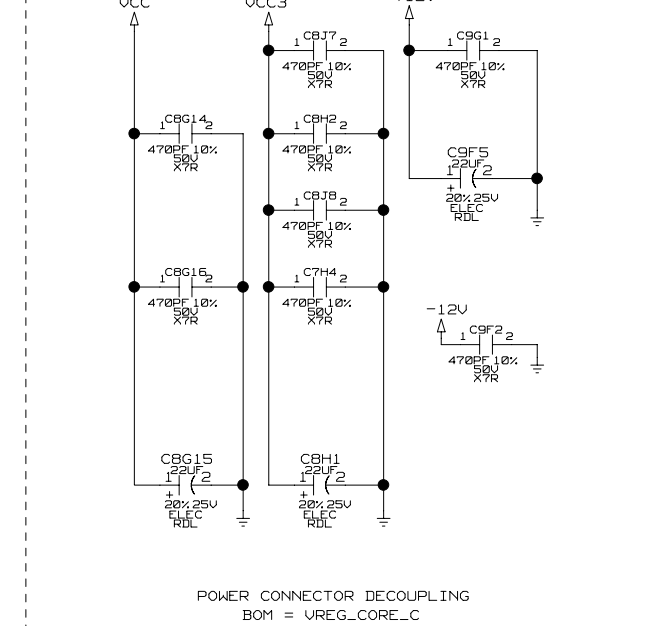
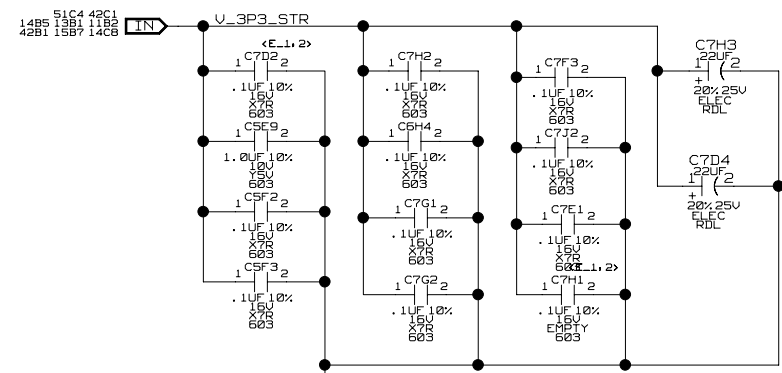


\* NOTE: PLACE ONE 4.7 UF AND TWO .1 UF  
DECOUPLING CAPS PER EACH SIDE OF 82559.  
PLACE DECOUPLING CAPS 130 MILS FROM 82559.

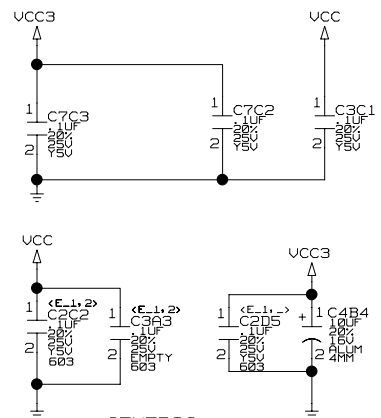
82559 LAN DECOUPLING



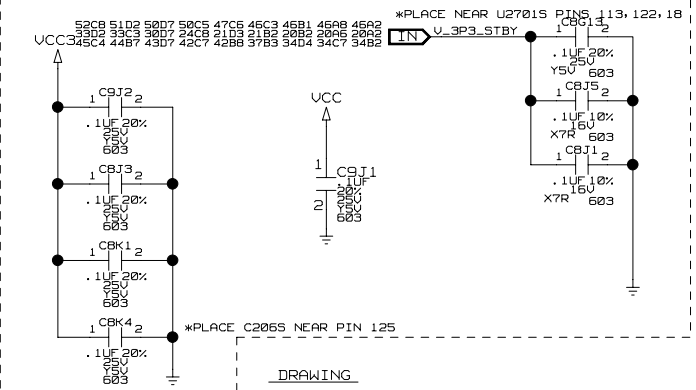
CICH DECOUPLING

POWER CONNECTOR DECOUPLING  
BOM = VREG\_CORE\_C

DIMM DECOUPLING



GENERIC



SIO DECOUPLING

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5000 W. CHANDLER BLVD  
CHANDLER, AZ 85226

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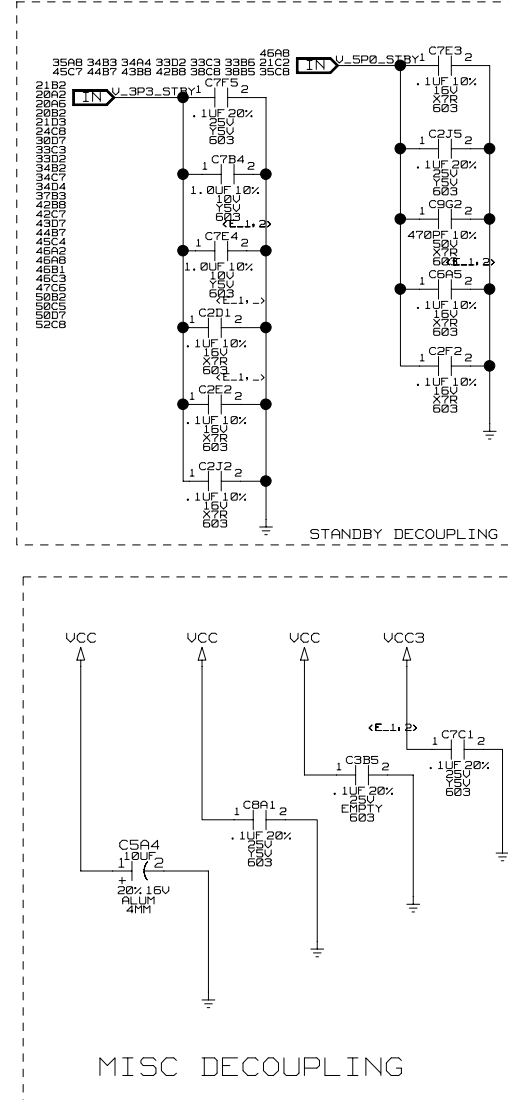
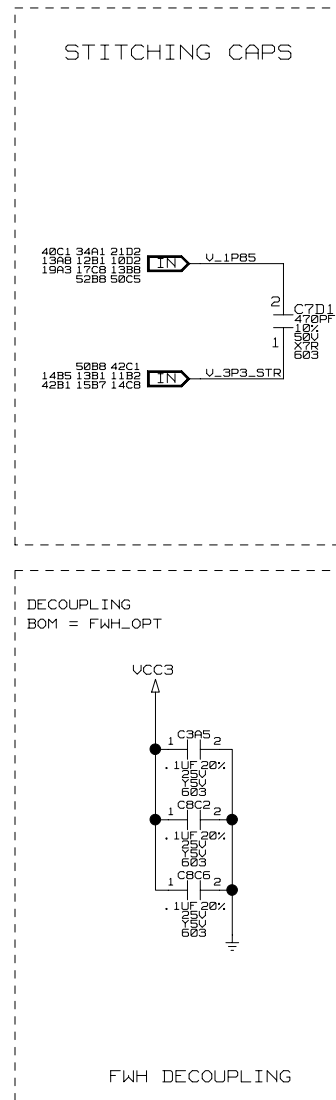
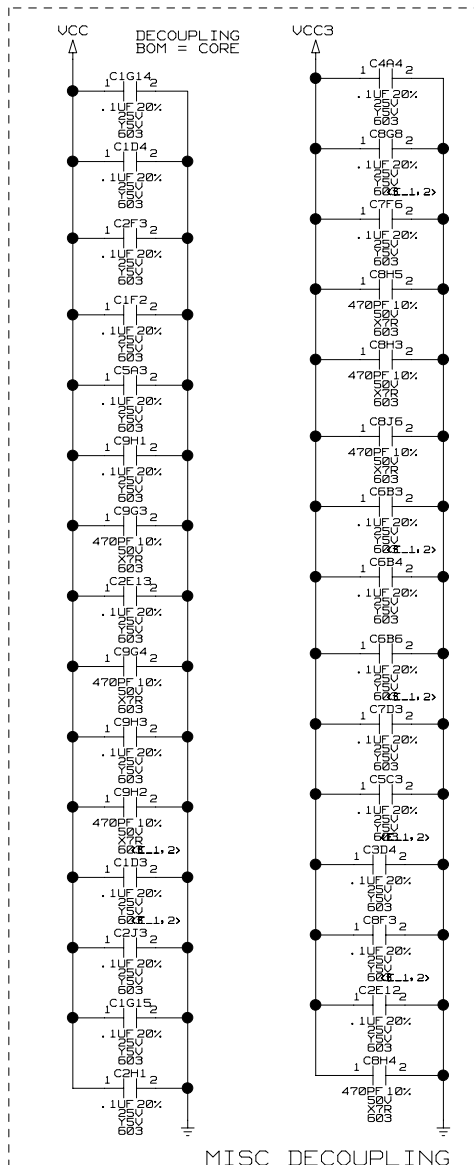
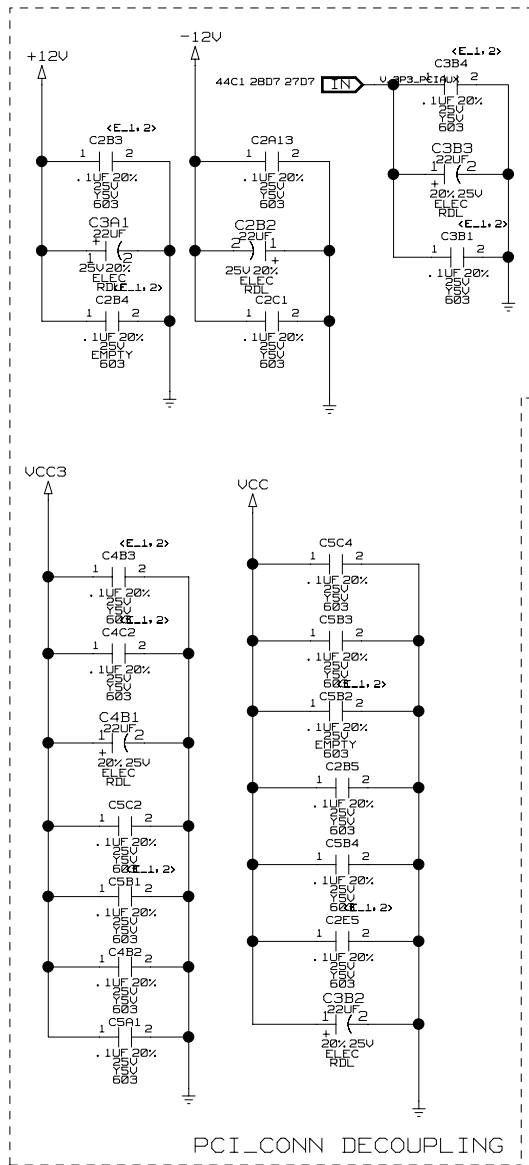
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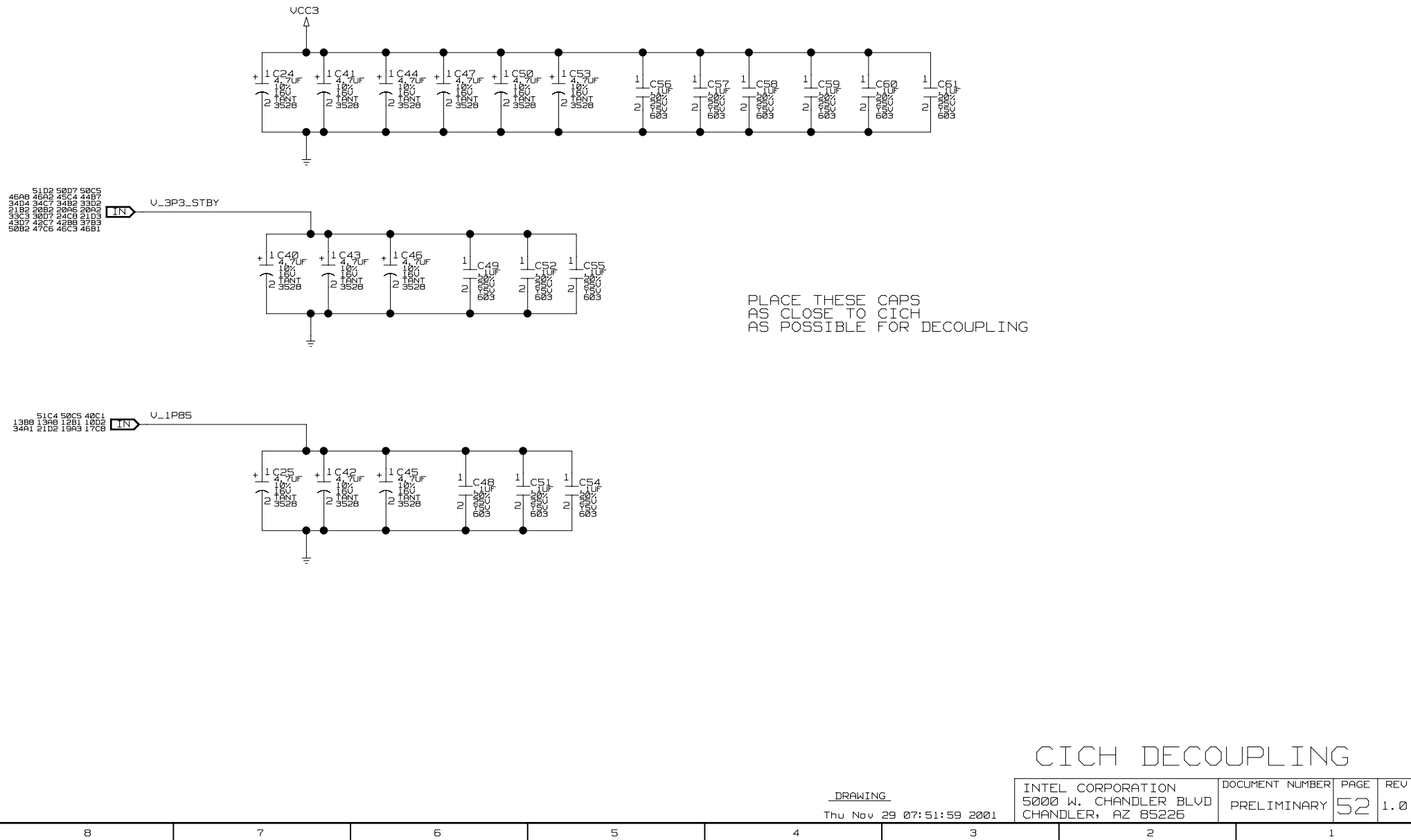
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CICH DECOUPLING

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